LCFC Confidential

L340-IRH +N18P MB Schematics Document

Coffee Lake-R with DDR4 + Nvidia N18P-G0

2018-09-21

REV:1.0

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

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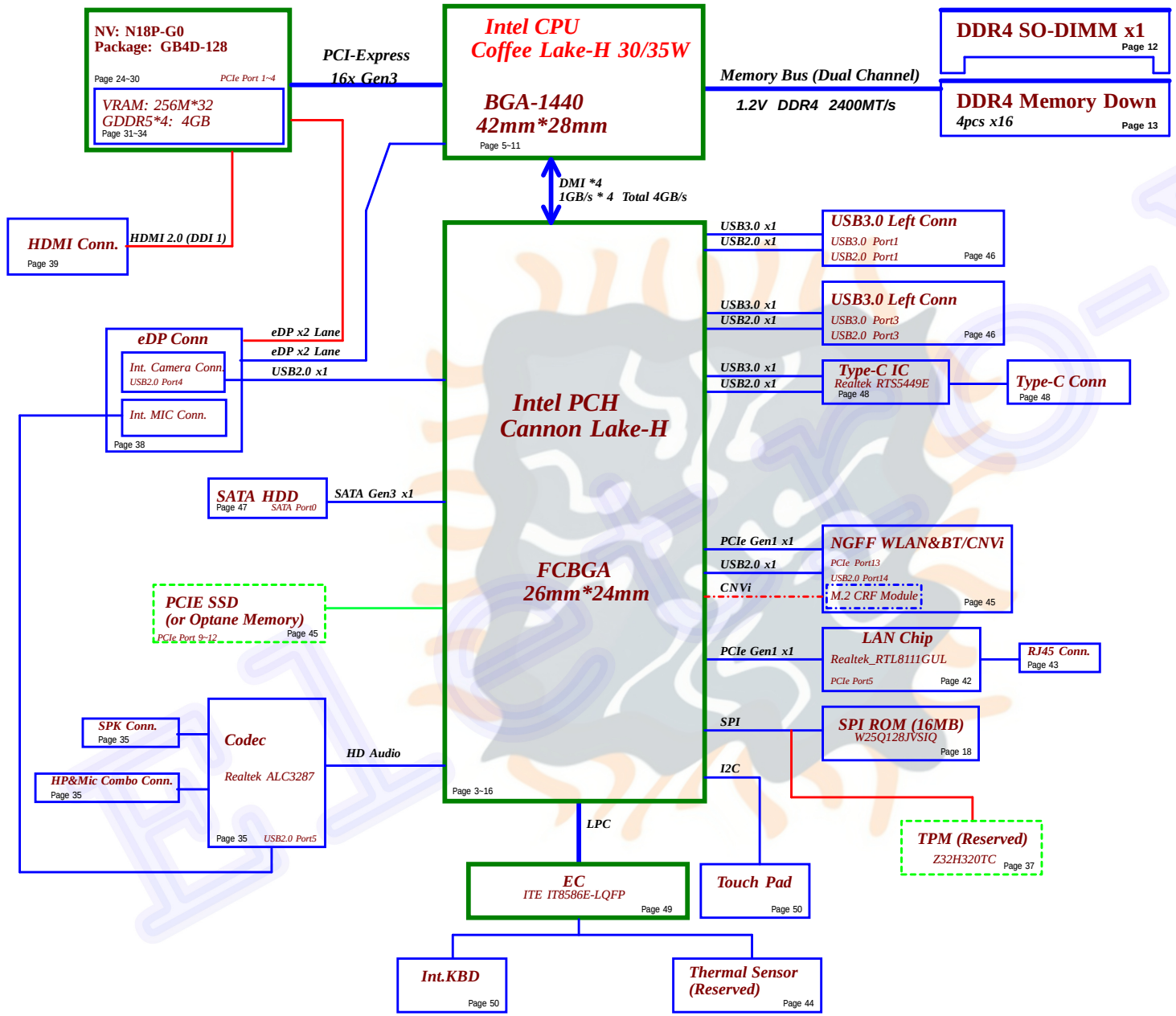
Title: *Cover Page*

Size: Custom | Document Number: *FG541/FG741* | Rev: 0.1

Date: Thursday, January 03, 2019 | Sheet 1 of 69

Eletro-X



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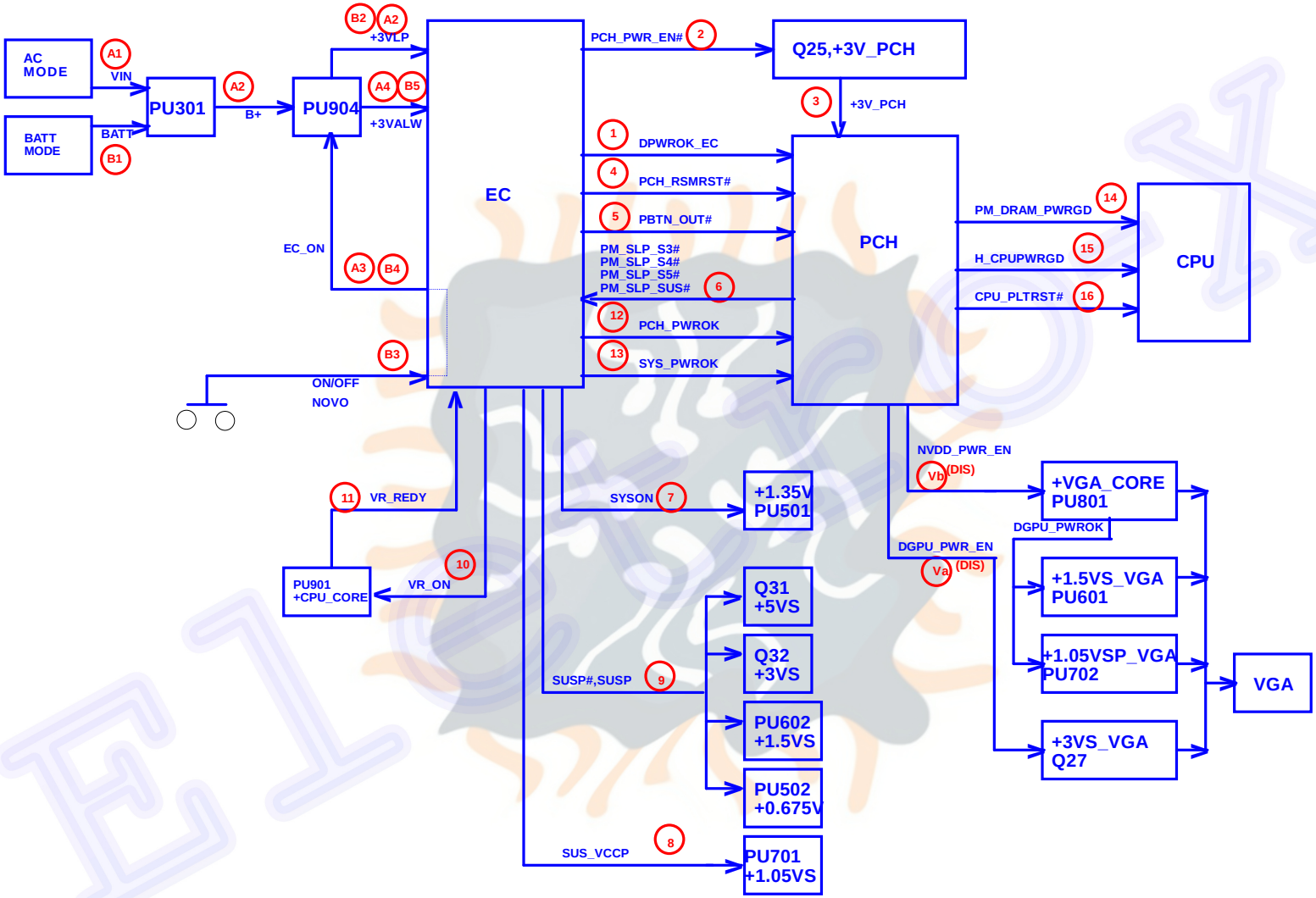
Title: Block Diagram

Size: Custom | Document Number: FG541/FG741 | Rev: 0.1

Date: Thursday, January 03, 2019 | Sheet 2 of 69

Eletro-X



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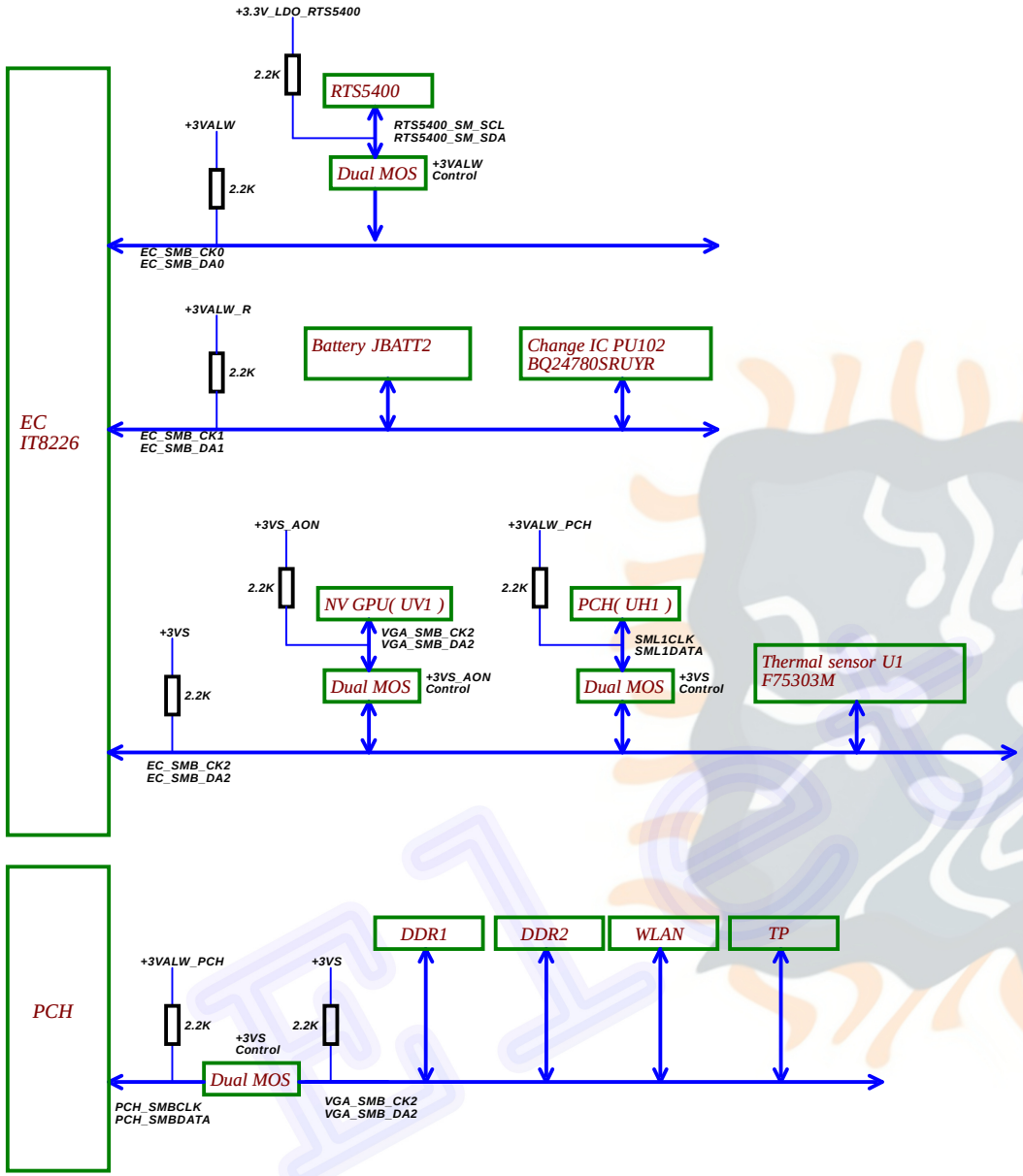
Title: **Power sequence block**

Size: Custom | Document Number: **FG541/FG741** | Rev: 0.1

Date: Thursday, January 03, 2019 | Sheet 52 of 69

Eletro-X



SMBUS Control Table

	SOURCE	VGA	BATT	IT8586E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1 EC_SMB_DA1	IT8226 +3VALW	X	V	V +3VALW	X	X	X	X	X	V
EC_SMB_CK2 EC_SMB_DA2	IT8226 +3VS	V +3VGS	X	V +3VS	X	X	V +3VS	V +3VALW_PCH	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X

EC SM Bus1 address

Device	
Smart Battery	0X16
Charger	0001 0010 b

EC SM Bus2 address

Device	Address
Thermal Sensor F75303M	1001_100xb
VGA	0x41(default)
PCH	need to update
RTS5400	0xD4

PCH SM Bus address

Device	Address
DDR DIMMA	1010 000Xb
DDR DIMMB	1010 010Xb
WLAN	Rsvd

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Title: Blank4

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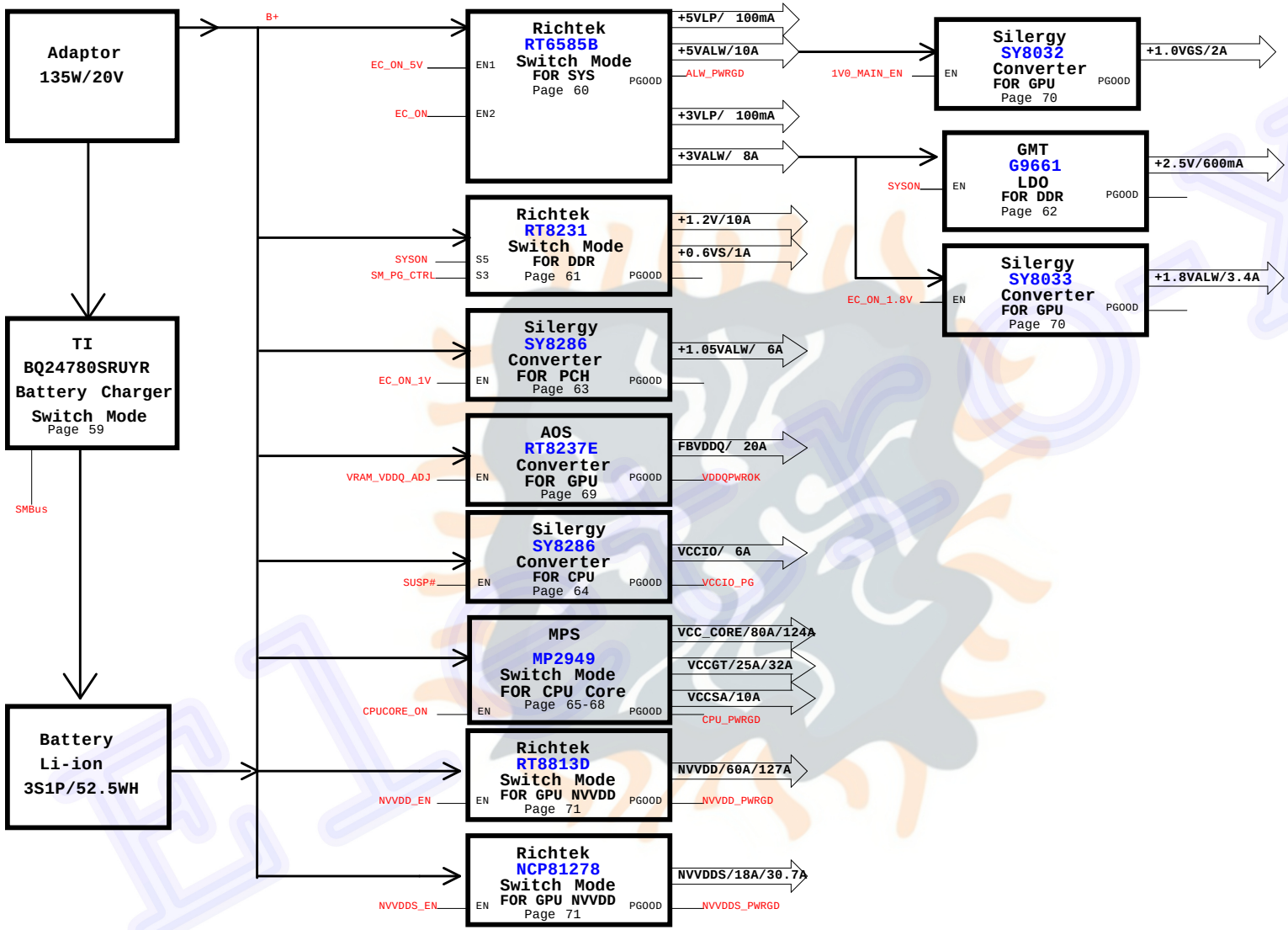
Date: Thursday, January 08, 2015 | Sheet 4 of 69

Eletro-X



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Title: **Power Diagram**

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Date: Wednesday, February 27, 2019 | Sheet 57 of 63

Eletro-X

Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL		SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT		Function
USB3.0	1	USB3.0 Conn Left
	2	USB Type-C
	3	USB3.0 Conn Left
	4	NC
	5	NC
	6	NC
USB2.0	1	USB3.0 Conn Left
	2	USB Type-C
	3	USB3.0 Conn Left
	4	Finger Print
	5	Cardreader
	6	Touch Panel
	7	Bluetooth
	8	Camera
	9	NC
	10	NC
PCIE	1~4 X4 PCIE	DGPU
	5	LAN
	6	WLAN
	7	SATA HDD
	8	SATA ODD
	9~12 X4 PCIE	Optane Memory
SATA	0	HDD
	1A	ODD
	1B	used as PCIE
	2	used as PCIE

BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
17@	For 17" part
15or17@	For 15" or 17" part
Cannonlake@	For Cannonlake part
CD@	For C cost down
DUALMIC@	For Dual MIC part
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC nu-stuff part
EMC_PX@	For EMC PX part
EMC_PXNS@	For EMC PX nu-stuff part
ES@	For ES CPU
EXO@	For EXO GPU
ME@	For ME part
TS@	For touch screen part
TS_NS@	For nu-touch part
DIS@	For GPU part
OPT@	For NV GPU part
PX@	For AMD GPU part
RANKA@	For VRAM rank A part
RANKB@	For VRAM rank B part
Realtek_SD@	For Realtek SD part
SINGLEMIC@	For single MIC part
SINGLERANK@	For single VRAN rank part
DUALRANK@	For dual VRAN rank part
TPM@	For TPM part
UMA@	For UMA part

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

EC SMBus1 address

Device	Address
Smart Battery	need to update
Charger	0001 0010 b

EC SMBus2 address

Device	Address
Thermal Sensor(NCT7718W)	1001_100xb
PCH	need to update
DGPU	need to update

EC SMBus3 address

Device	Address
PMIC	need to update

PCH SM Bus address

Device	Address
DDR4 SODIMM	need to update
Wlan	Reserved

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Title: Notes List

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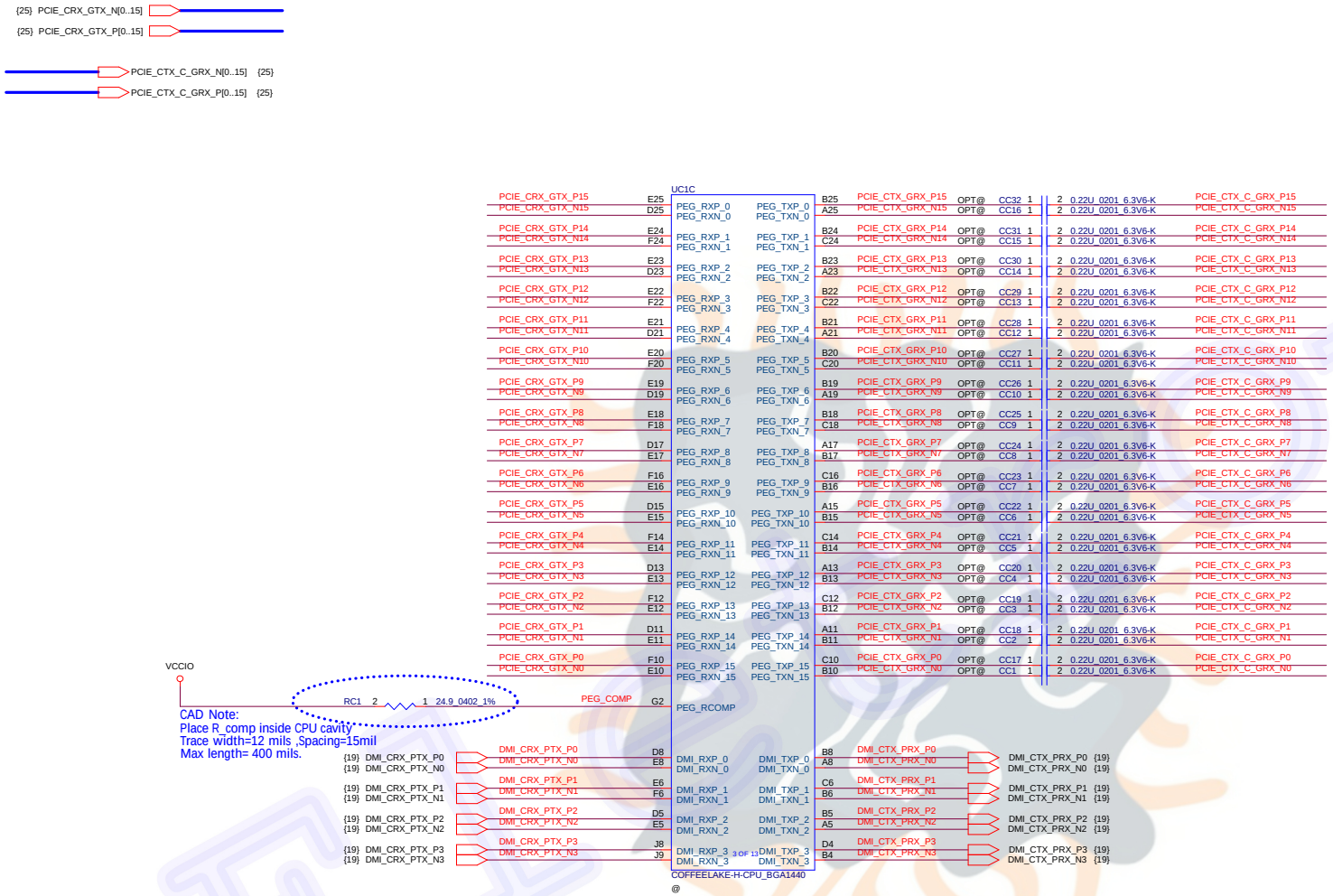
Date: Thursday, January 03, 2019 | Sheet 3 of 69

Eletro-X



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Title: CPU (1/7) DMI,PEG

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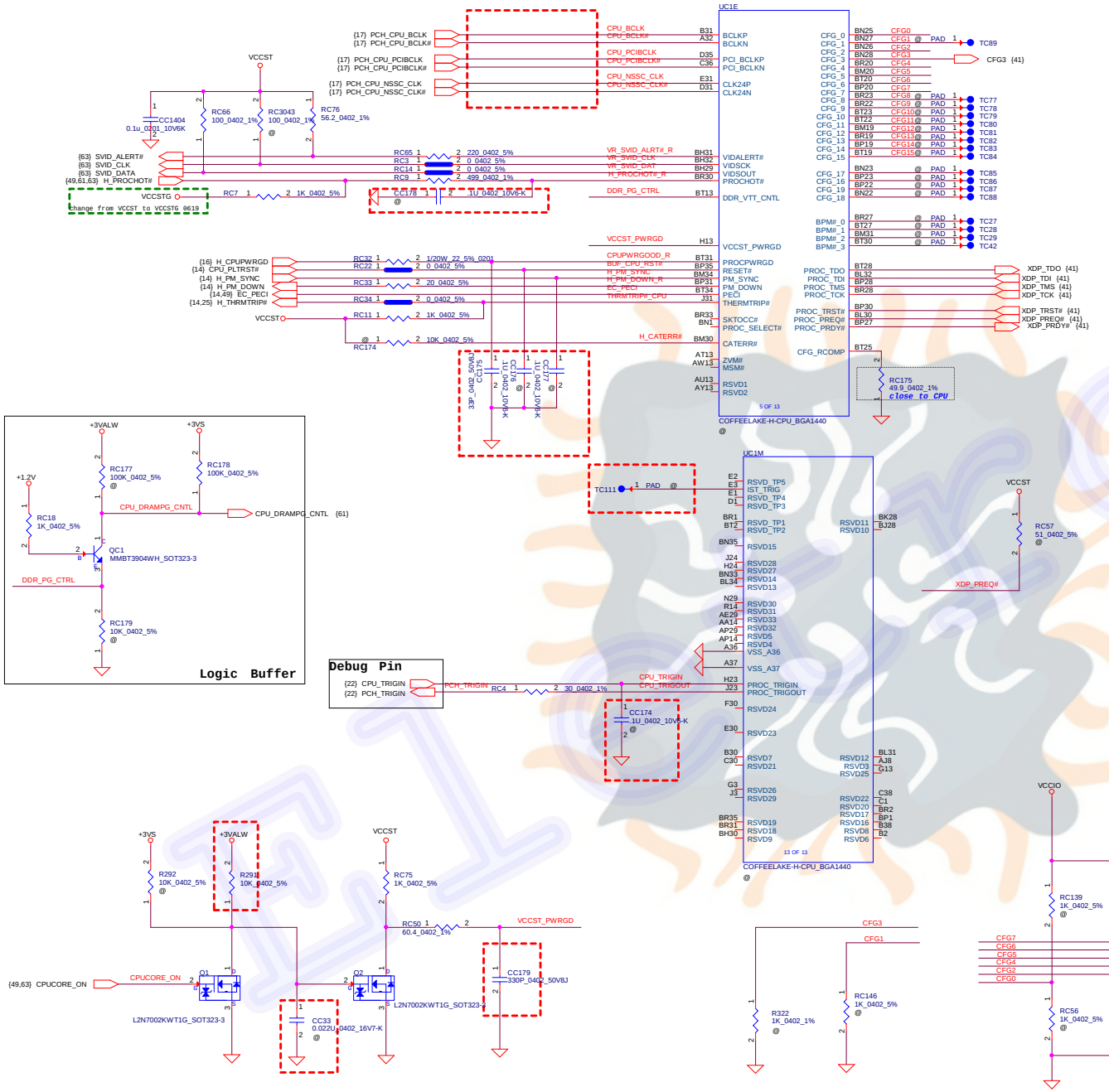
Date: Thursday, January 03, 2019 | Sheet 5 of 69

Eletro-X



CFG STRAPS for CPU

Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	* 1 = (Default) Normal Operation; No stall. 0 = Stall.

Reserved configuration lane	
CFG1	N/A

PCI Express* Static x16 Lane Numbering Reversal	
CFG2	☐ 1 = Normal operation *☐ 0 = Lane numbers reversed.

Reserved configuration lane.	
CFG3	N/A

eDP enable	
CFG4	1 = Disabled. * 0 = Enabled.

PCI Express* Bifurcation	
CFG[6:5]	00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* * 11 = 1 x16 PCI Express*

PEG Training	
CFG7	* 1 = (default) PEG Train immediately following RESET# deassertion. 0 = PEG Wait for BIOS for training.

Reserved configuration lane.	
CFG[19:8]	N/A

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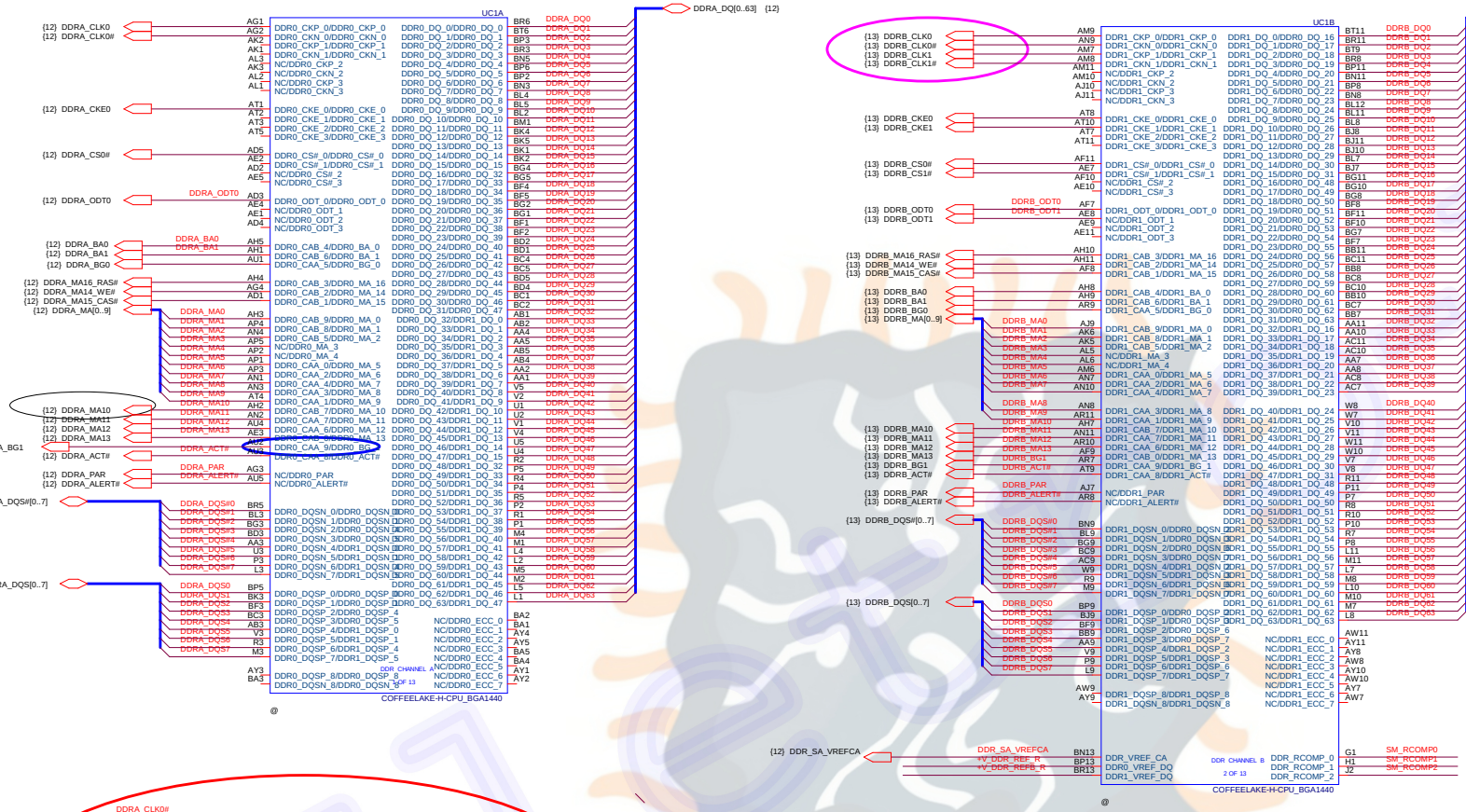
Title: CPU (2/7) PM, XDP, CLK, CFG

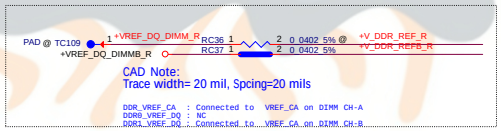
Size: Custom | Document Number: FG541/FG741 | Rev: 0.1

Date: Thursday, January 24, 2019 | Sheet 6 of 69

Eletro-X



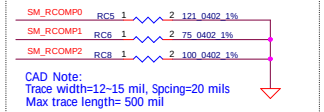
Follow 1.0PDG to reserve 3.3P_0201 capacitor between DDRA_CLK0 and DDRA_CLK0# --SF0904



CAD Note:
Trace width= 20 mil, Spcing=20 mils

DDR_VREF_CA : Connected to VREF_CA on DIMM CH-A
DDR0_VREF_DQ : NC
DDR1_VREF_DQ : Connected to VREF_CA on DIMM CH-B

DDR4 COMPENSATION SIGNALS



CAD Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mil

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Title: CPU (3/7) DDRVI

Size: C | Document Number: FG541/FG741 | Rev: 0.1

Date: Thursday, January 03, 2019 | Sheet 7 of 69

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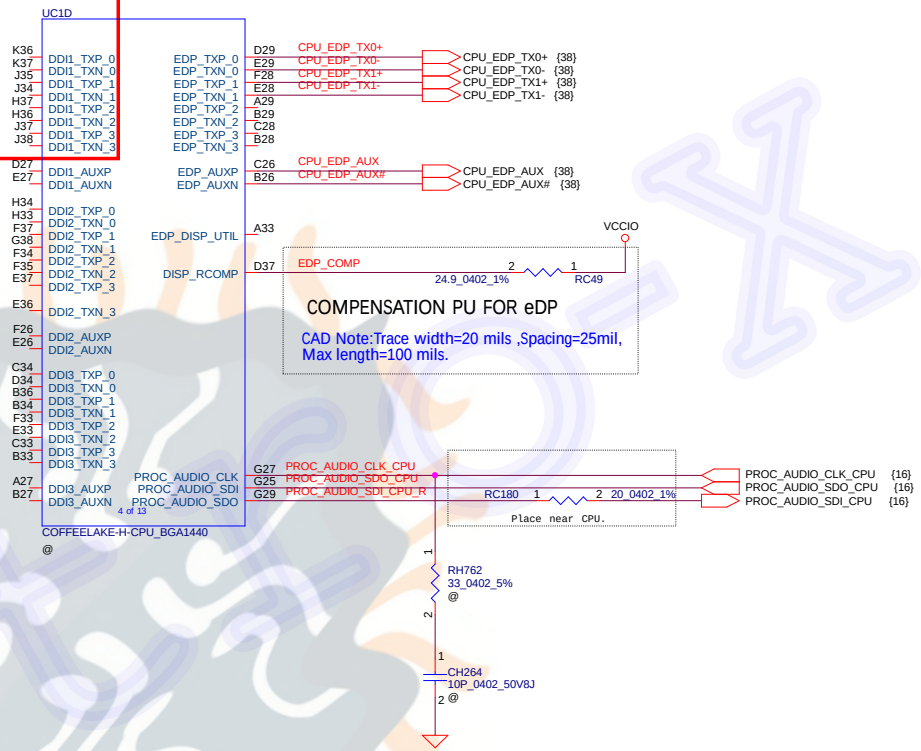
change HDMI DDI from CPU to GPU



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Title: CPU (4/7) eDP, DDI

Size: A3 | Document Number: FG541/FG741 | Rev: 0.1

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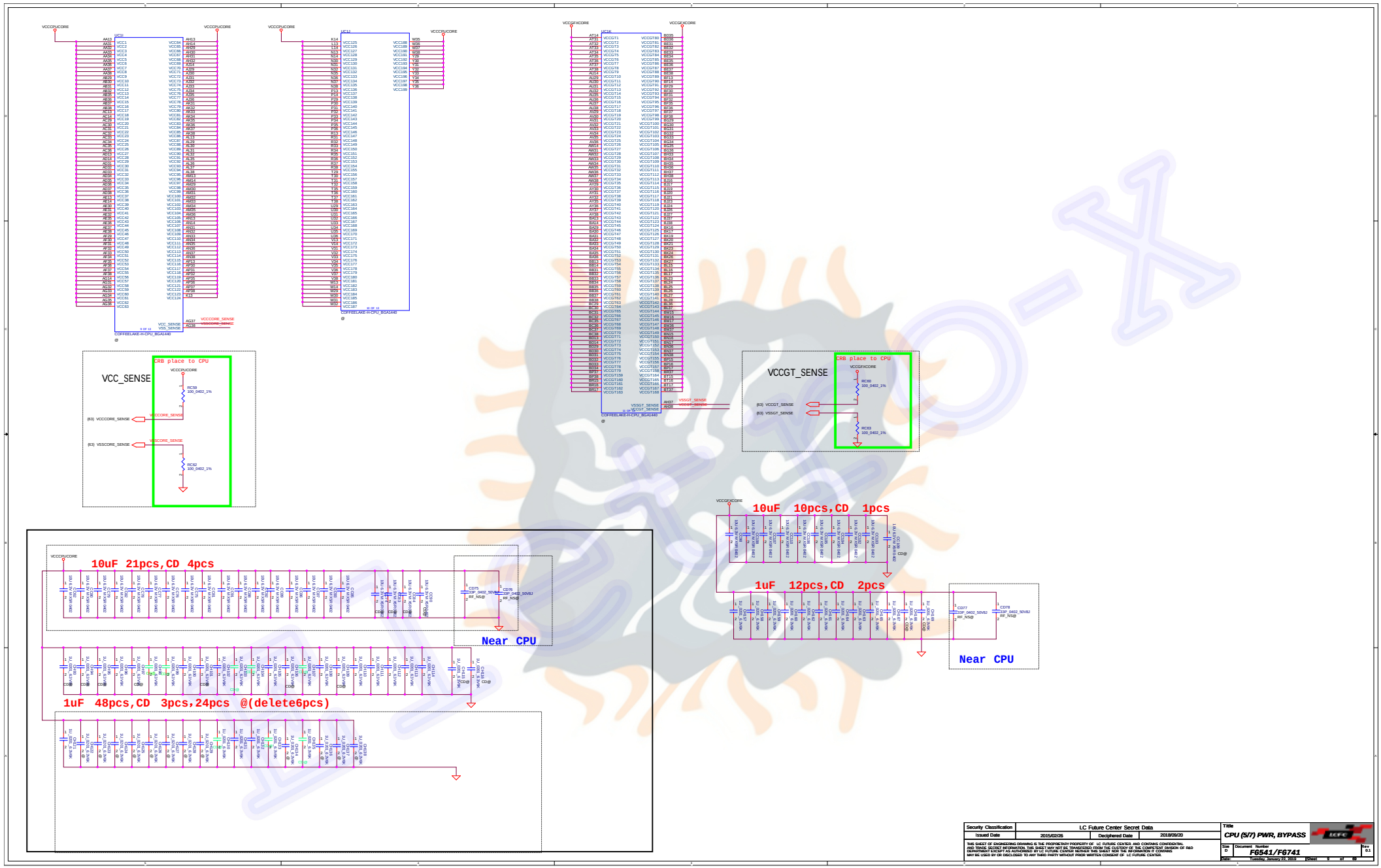
Eletro-X


VCC_SENSE
CRB place to CPU
VCCGT_SENSE
CRB place to CPU
10uF 21pcs,CD 4pcs
Near CPU
1uF 48pcs,CD 3pcs,24pcs @(delete6pcs)
10uF 10pcs,CD 1pcs
1uF 12pcs,CD 2pcs
Near CPU
Security Classification
LC Future Center Secret Data
Issued Date
2015/02/26
Deciphered Date
2018/09/20
Title
CPU (5/7) PWR, BYPASS
Size
D
Document Number
F6541/F6741
Rev
0.1
Date: Tuesday, January 17, 2023
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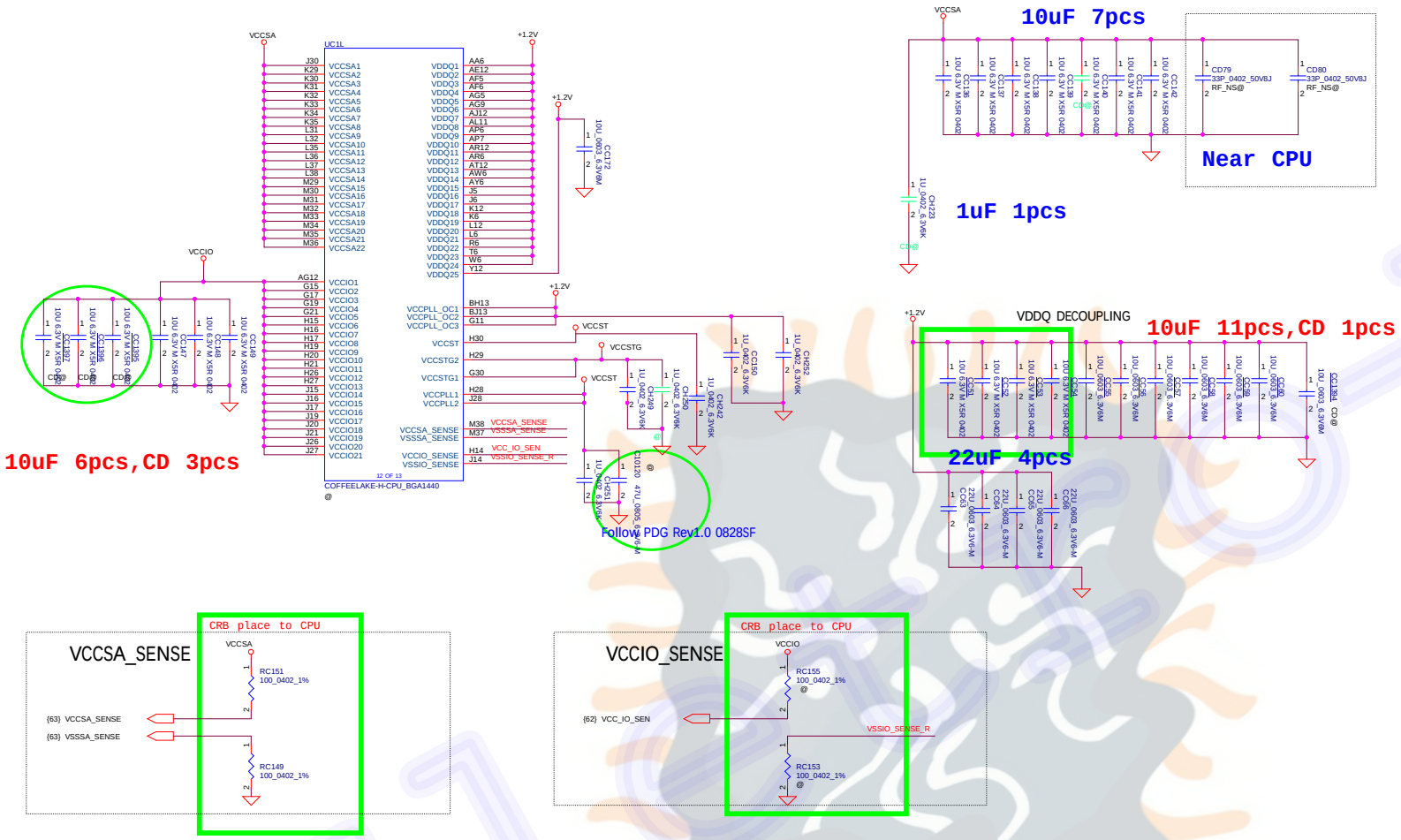
Eletro-X



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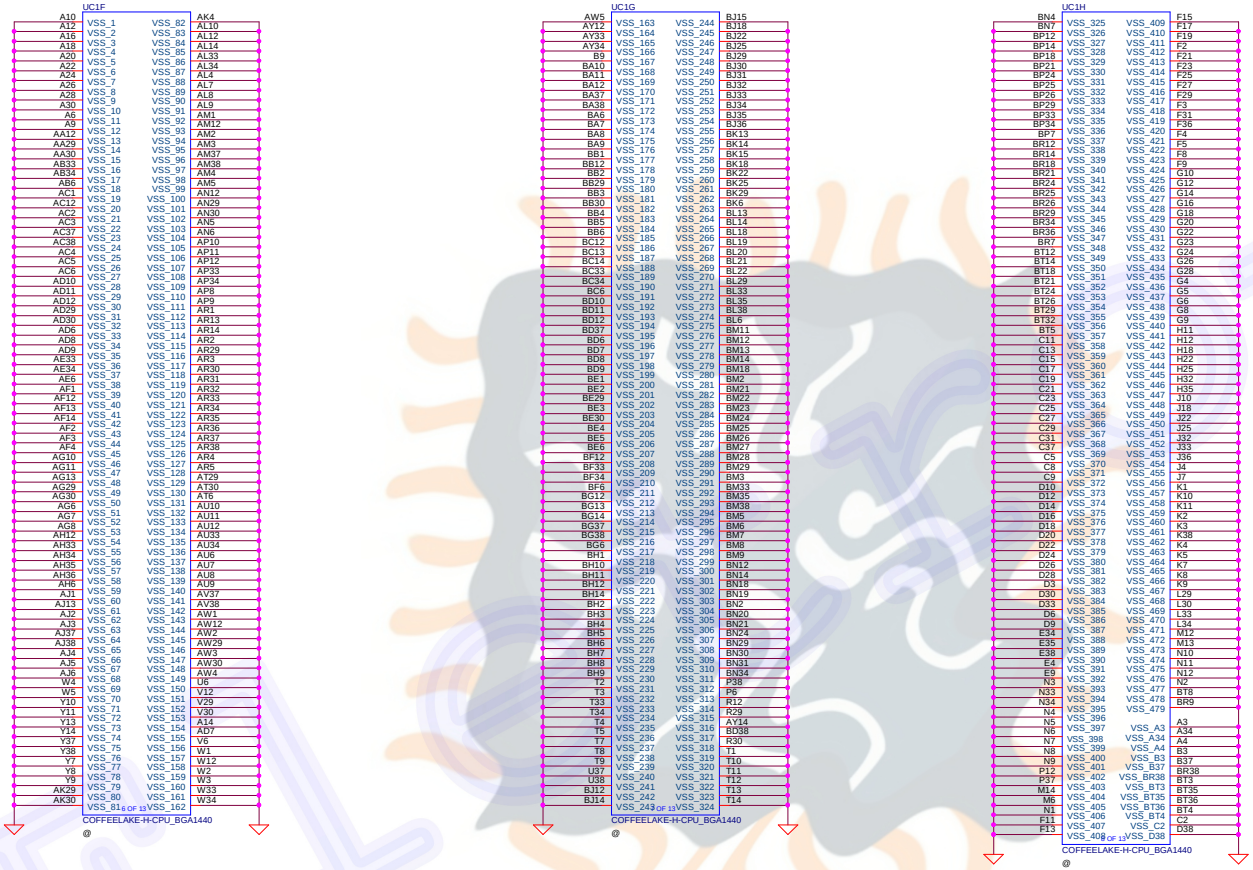
Title: CPU (6/7) PWR, BYPASS

Size: C | Document Number: FG541/FG741 | Rev: 0.1

Date: Saturday, February 02, 2019 | Sheet 10 of 69

Eletro-X



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Title

CPU (6/7) PWR, VSS

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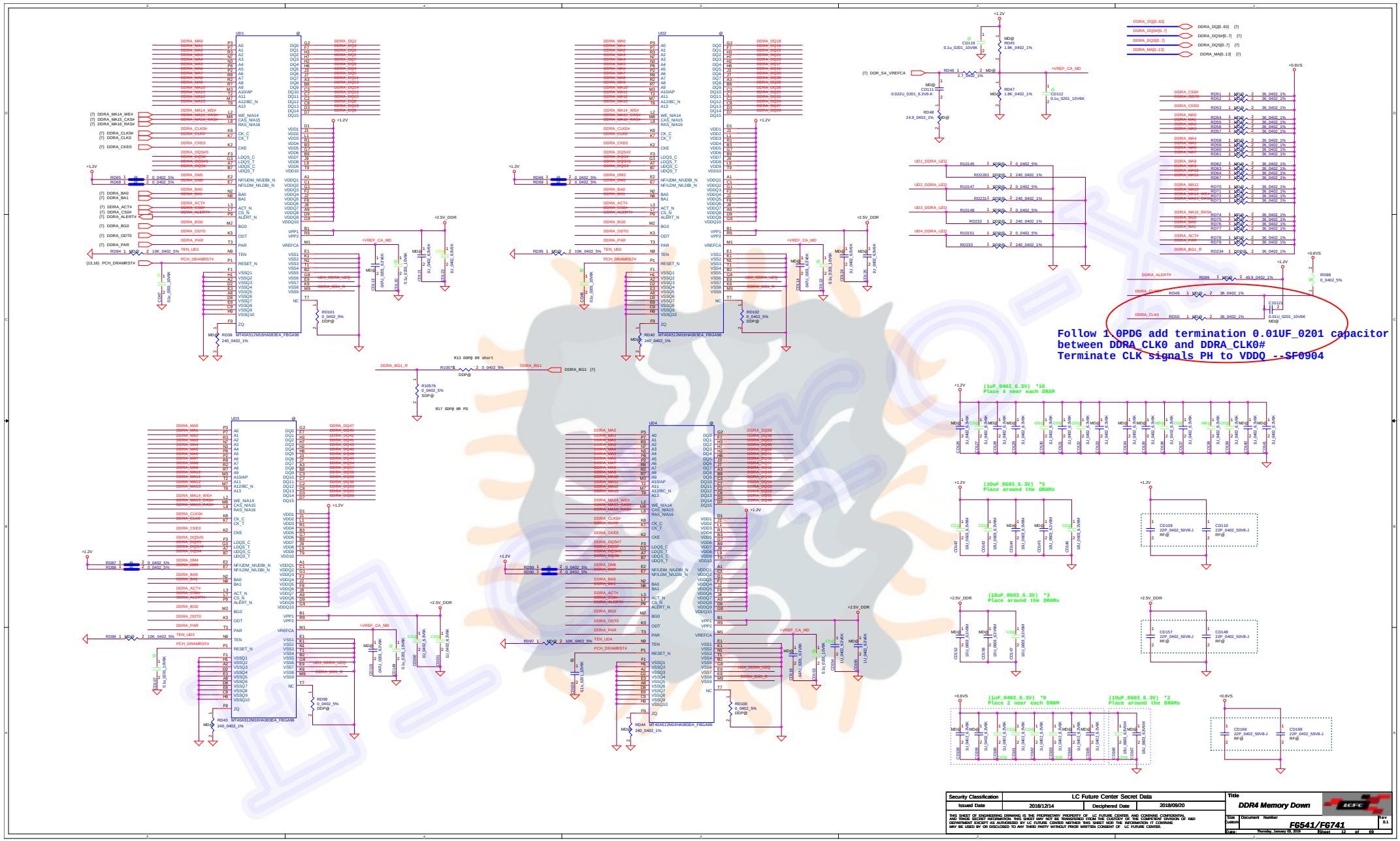
UD1
UD2
UD3
UD4
MT40A512M16HA083EA_FBGA96
Follow 1.0PDG add termination 0.01UF_0201 capacitor
between DDRA_CLK0 and DDRA_CLK0#
Terminate CLK signals PH to VDDQ --SF0904
(1uF_0402_6.3V) *16
Place 4 near each DRAM
(10uF_0603_6.3V) *5
Place around the DRAMs
(10uF_0603_6.3V) *3
Place around the DRAMs
(1uF_0402_6.3V) *8
Place 2 near each DRAM
(10UF_0603_6.3V) *2
Place around the DRAMs
Security Classification
LC Future Center Secret Data
Issued Date
2016/12/14
Deciphered Date
2018/09/20
Title
DDR4 Memory Down
Size
Document Number
FG541/FG741
Rev
0.1
Date: Thursday, January 31, 2019
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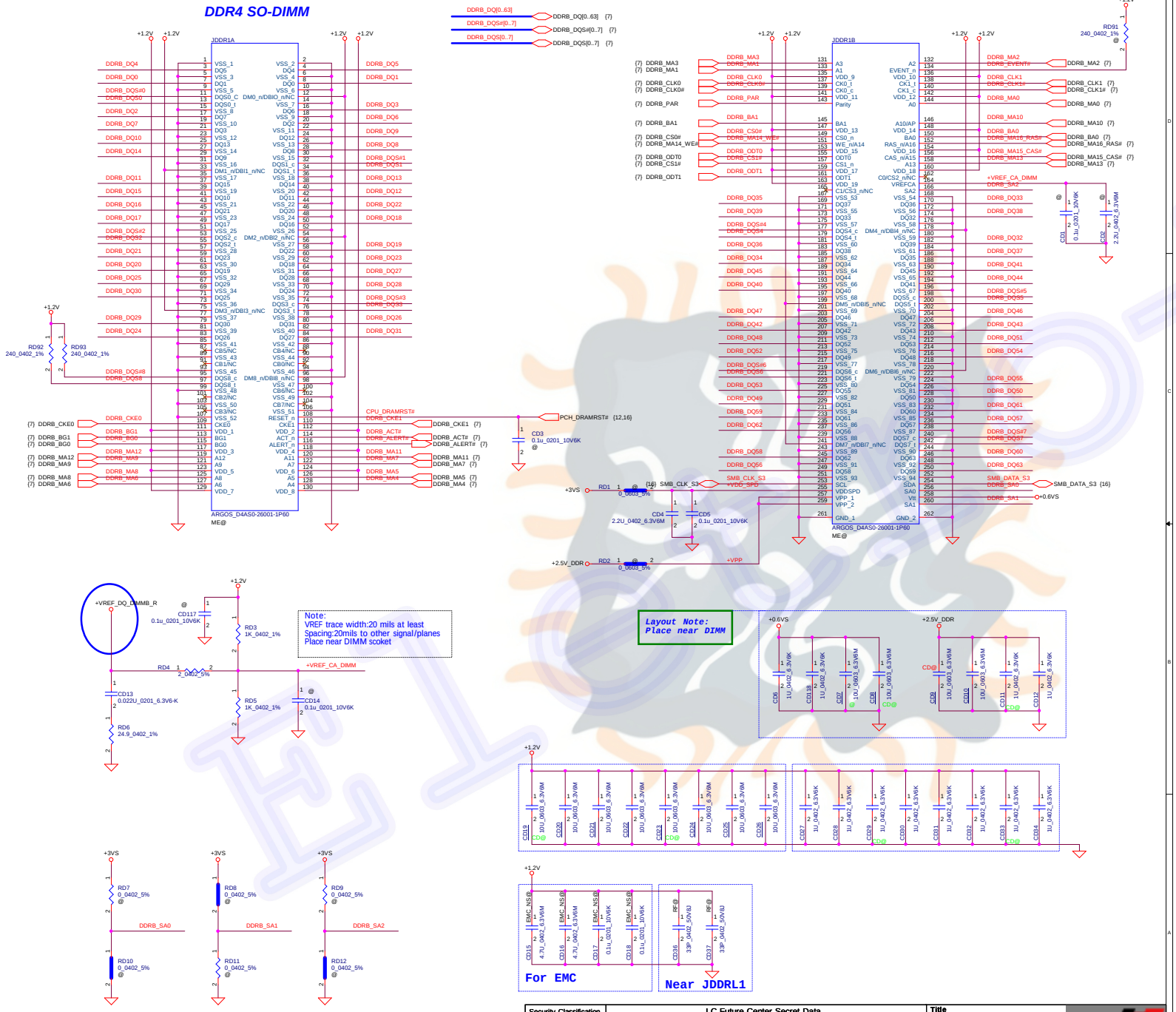
Eletro-X

DDR4 SO-DIMM



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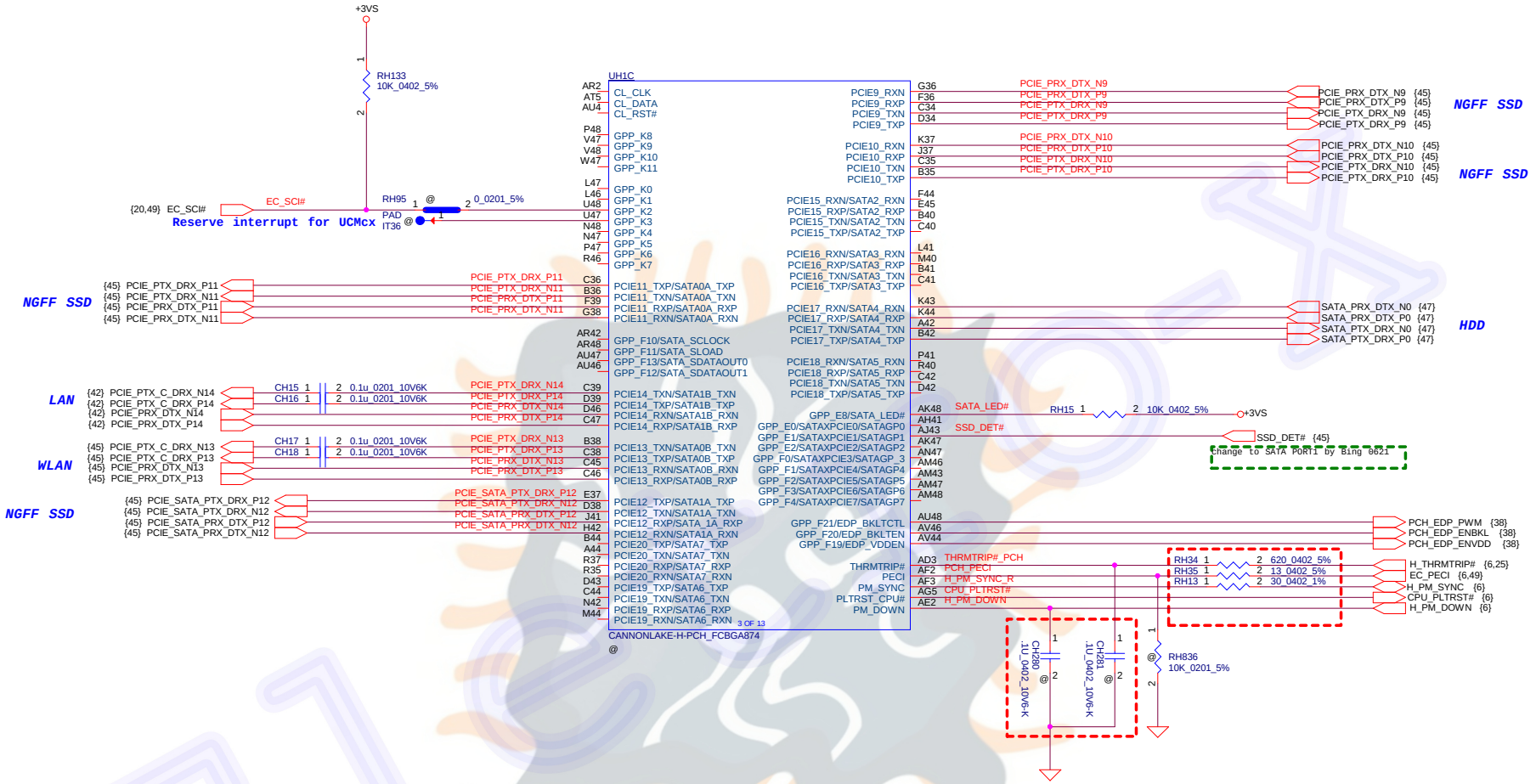
Title: DDR4 SO-DIMM

Size: Custom | Document Number: FG541/FG741 | Rev: 0.1

Date: Tuesday, January 22, 2019 | Sheet 13 of 69

Eletro-X



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Title: PCH (1/9) PCIe/SATA/GPPFG

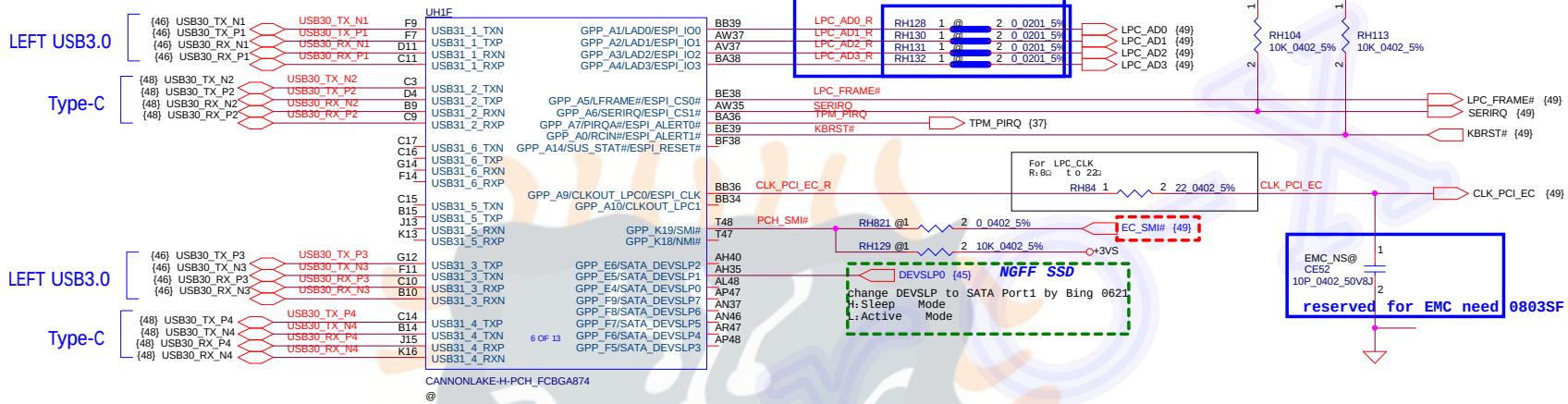
Size: A3 | Document Number: FG541/FG741 | Rev: 0.1

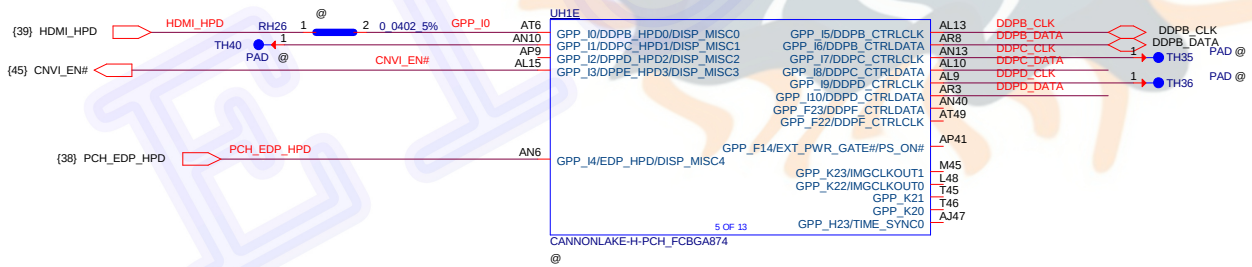
Date: Tuesday, February 26, 2019 | Sheet 14 of 69

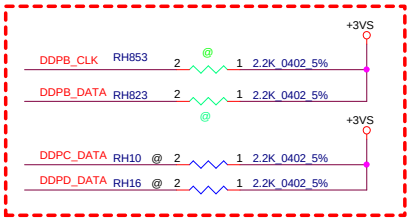
Eletro-X

HM370 only have 4(#1-#4) USB3.1 GEN2 port

Follow PDG add R/C 1010SF close to PCH







DDPB_CTRLDATA
The signal has a weak internal pull-down.
H Port B is detected.
L Port B is not detected.

DDPC_CTRLDATA
The signal has a weak internal pull-down.
H Port C is detected.
L Port C is not detected. (Default)

DDPD_CTRLDATA
The signal has a weak internal pull-down.
H Port D is detected.
L Port D is not detected. (Default)

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Issued Date	2015/02/26	Deciphered Date	2018/09/20

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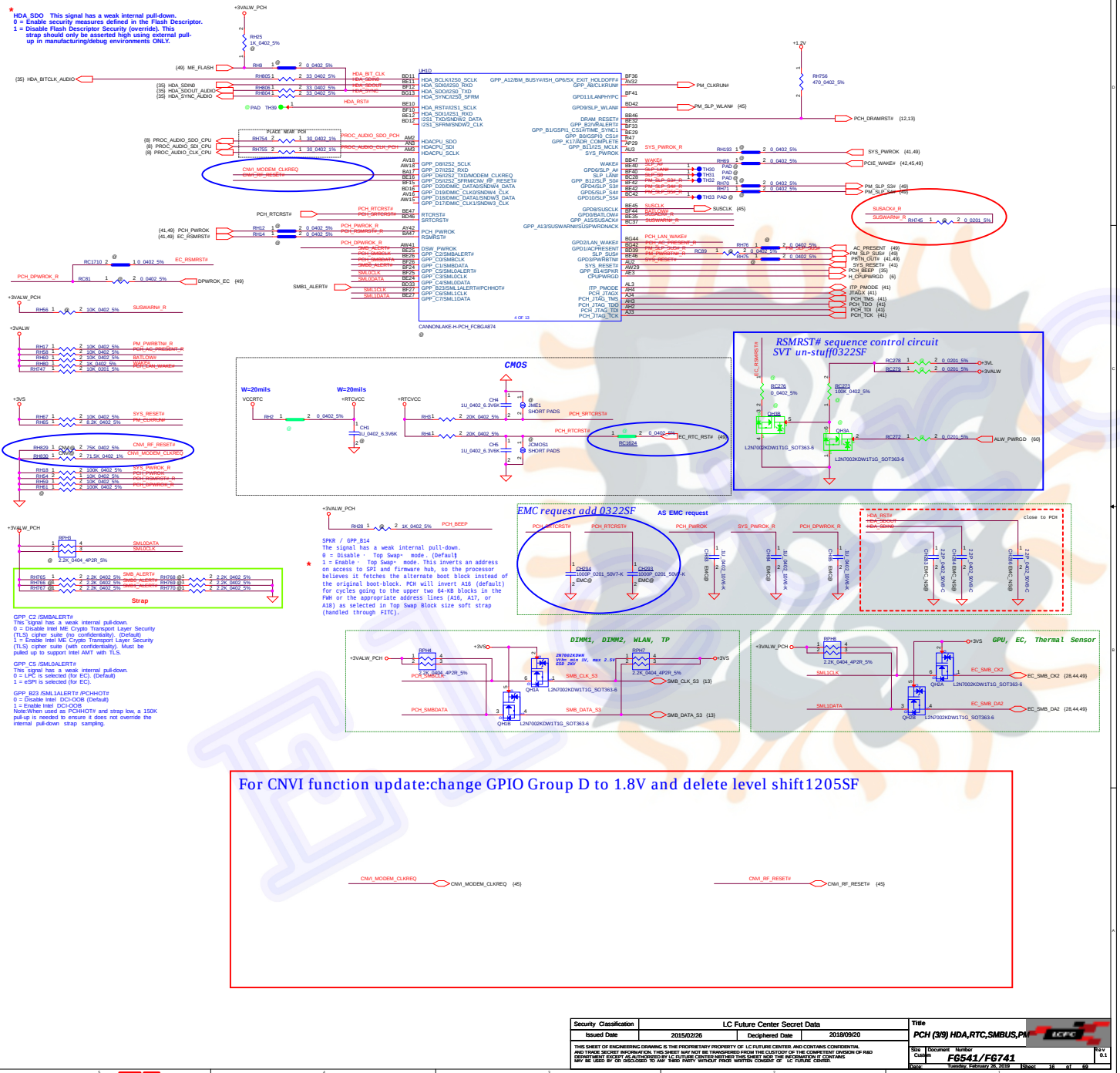
Title: PCH (2/9) USB3/GPPAEFGHI

Size A3 | Document Number: FG541/FG741 | Rev 0.1

Date: Tuesday, February 26, 2019 | Sheet 15 of 69

Eletro-X


HDA_SDO This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
CMOS
W=20mils
W=20mils
RSMRST# sequence control circuit
SVT un-stuff0322SF
EMC request add 0322SF
AS EMC request
close to PCH
SPKR / GPP_B14
The signal has a weak internal pull-down.
0 = Disable · Top Swap· mode. (Default)
1 = Enable · Top Swap· mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (handled through FITC).
Strap
GPP_C2 /SMBALERT#
This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.
GPP_C5 /SML0ALERT#
This signal has a weak internal pull-down.
0 = LPC is selected (for EC). (Default)
1 = eSPI is selected (for EC).
GPP_B23 /SML1ALERT#/PCHHOT#
0 = Disable Intel DCI-OOB (Default)
1 = Enable Intel DCI-OOB
Note:When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling.
DIMM1, DIMM2, WLAN, TP
GPU, EC, Thermal Sensor
For CNVI function update:change GPIO Group D to 1.8V and delete level shift1205SF
CNVI_MODEM_CLKREQ
CNVI_RF_RESET#
Security Classification
LC Future Center Secret Data
Issued Date
2015/02/26
Deciphered Date
2018/09/20
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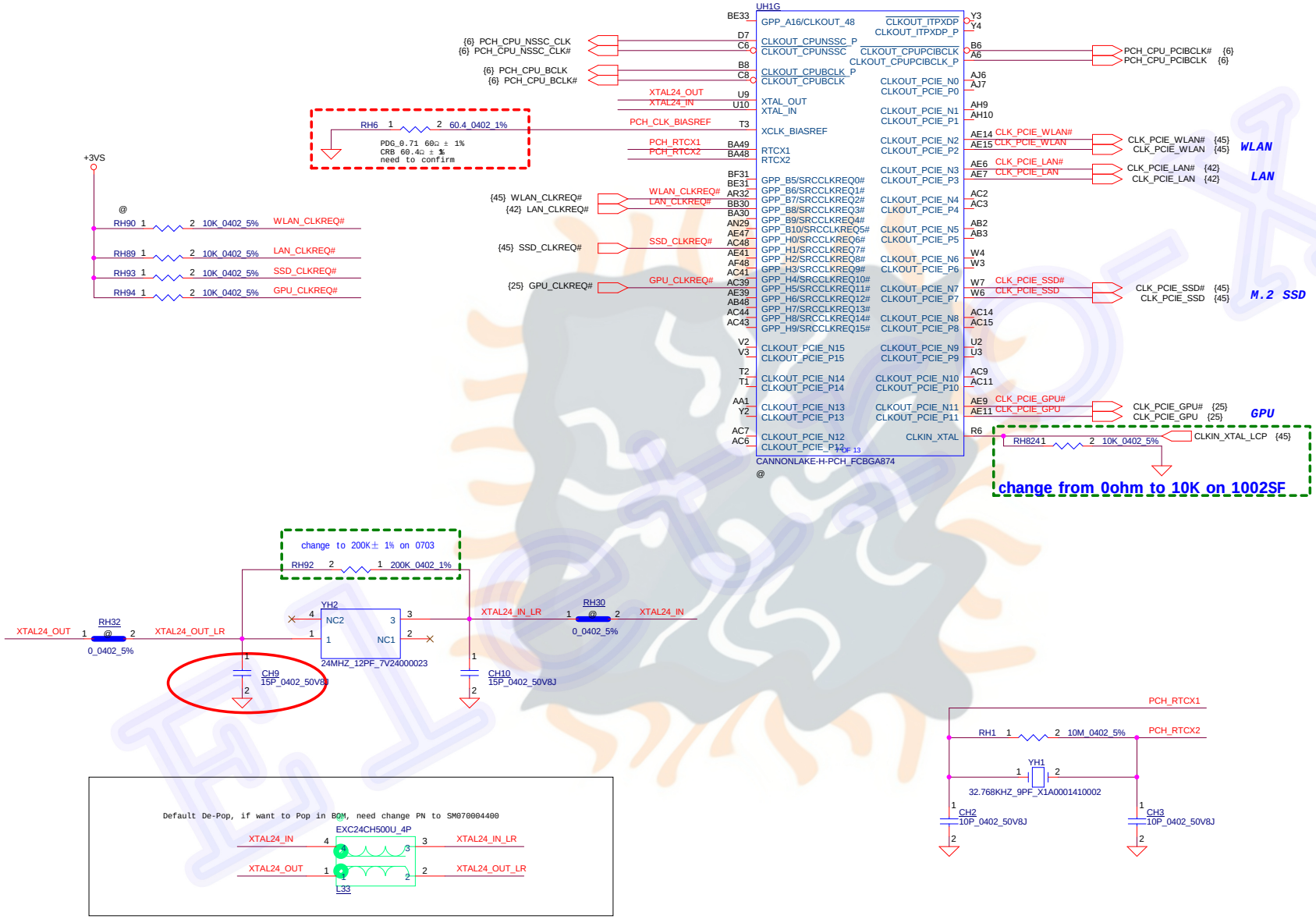
Title
PCH (3/9) HDA,RTC,SMBUS,PM
Size
Document Number
FG541/FG741
Rev
0.1
Date: Tuesday, February 26, 2019
Sheet 16 of 69

Eletro-X



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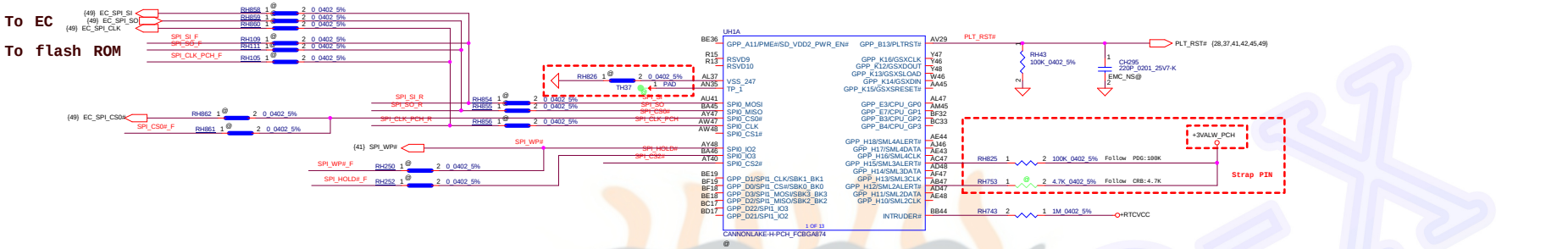
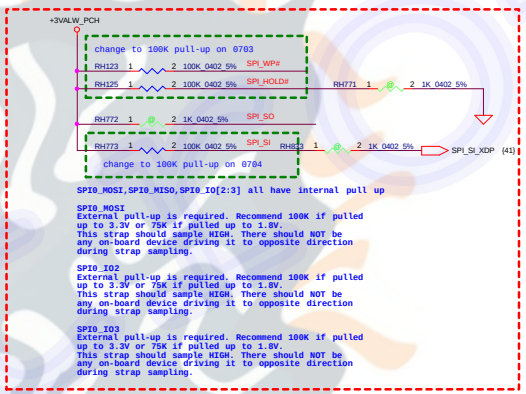
Title: PCH (3/9) CLOCK,GPPBH

Size: A3 | Document Number: FG541/FG741 | Rev: 0.1

Date: Tuesday, February 26, 2019 | Sheet 17 of 69

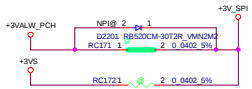
Eletro-X





GPP_H15 /SML3ALERT# (Strap reserved)
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
Power Plane: Primary Well

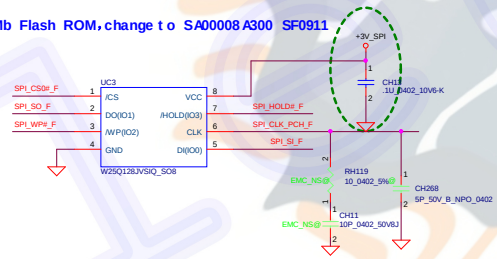
GPP_H12 /SML2ALERT#
This signal has a weak internal pull-down.
0 = Master Attached Flash Sharing (MAFS) enabled (Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.
Warning: This strap must be configured to ' 0' (SAFS is disabled) if the eSPI or LPC strap is configured to ' 0' (eSPI is disabled)
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.



+3V_SPI

* 1. If support DS3, connect to +3VS and don't support EC mirror code;
2. If don't support DS3, connect to +3VALW_PCH and support EC mirror code.

128Mb Flash ROM，change t o SA00008A300 SF0911



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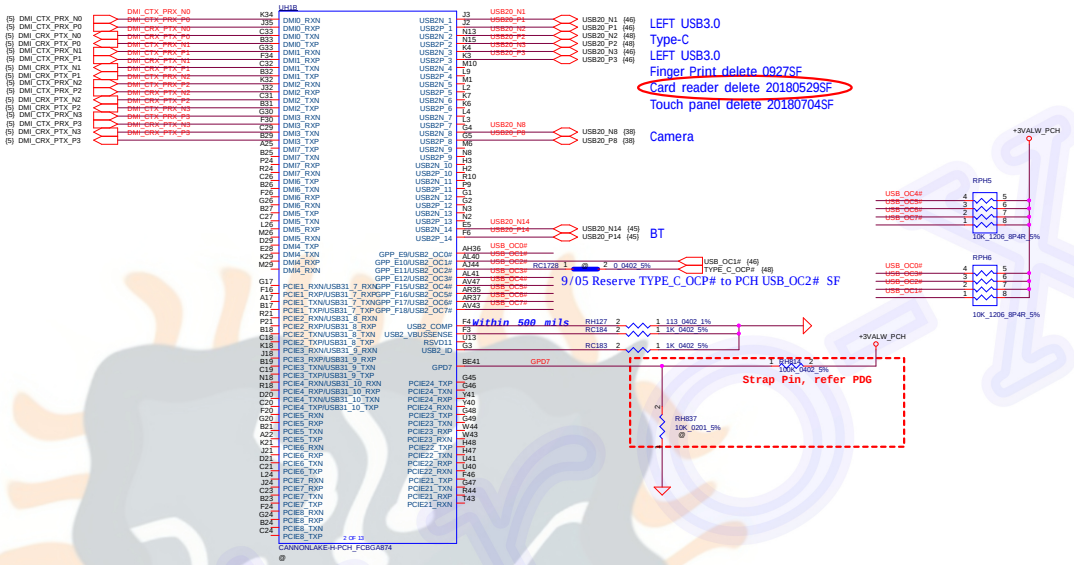
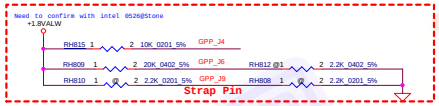
Title: PCH (5/9) SPI,SMBUS,GPPBEGH

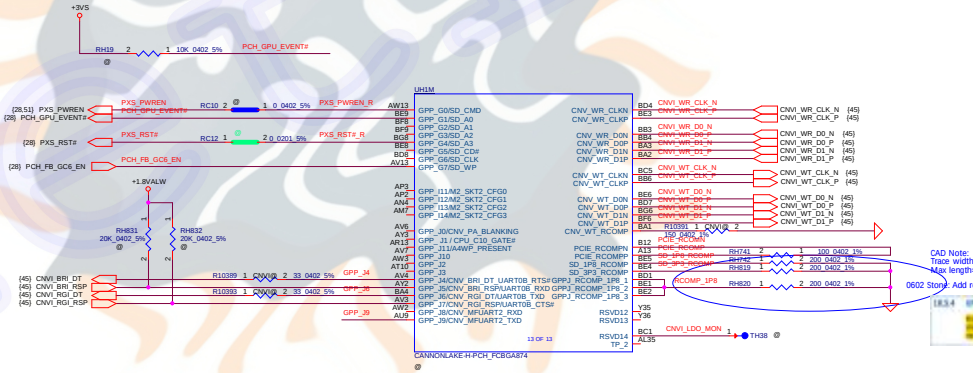
Size: A2 | Document Number: FG541/FG741 | Rev: 0.1

Date: Tuesday, February 26, 2019 | Sheet 18 of 69

Eletro-X







Primary Well Group J (1.8 V Only)

Signal	Usage	When Sampled	Comment
GPP_J4 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_J6 / CNV_RGI_DT / UART0_TXD	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.
GPP_J9	1.8V VCCSPI	Rising edge of RSMRST#	The signal has a weak internal pull-down 0 = VCCSPI is connected to 3.3V rail 1 = VCCSPI is connected to 1.8V rail **Note:** If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os

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Issued Date	2015/02/26	Deciphered Date	2018/09/20

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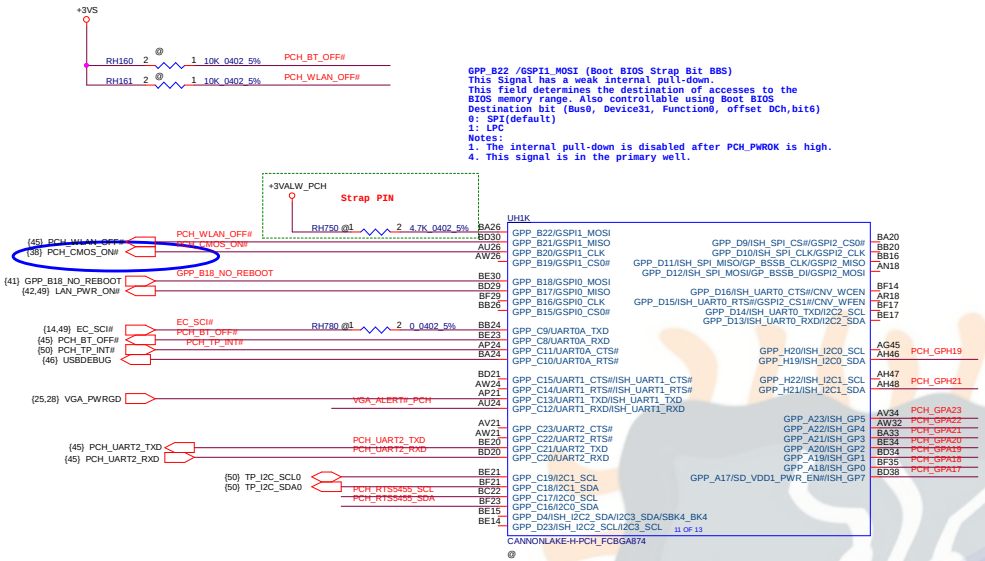
Title: Blank

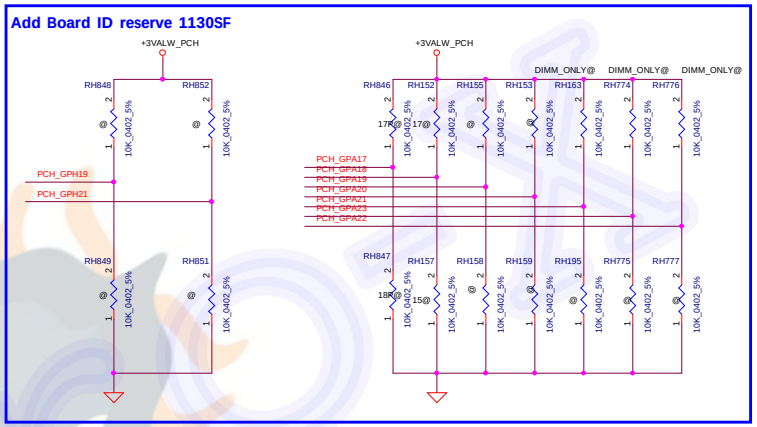
Size: Custom | Document Number: FG541/FG741 | Rev: 0.1

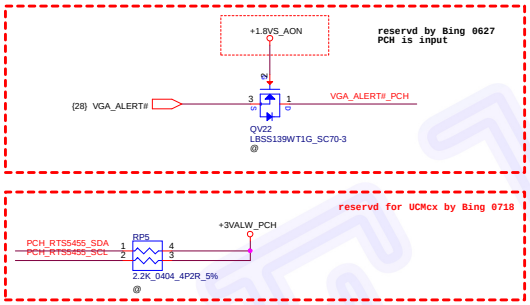
Date: Tuesday, February 26, 2019 | Sheet 19 of 69

Eletro-X



Bit 6	Boot BIOS Destination
0	SPI (Default)
1	LPC





SKU ID

Board ID	Description		Stuff R
PCH_GPA18	0	15" EG530	RH157
	1	17" EG730	RH152
PCH_GPA19	0	non-touch	RH158
	1	touch	RH155
PCH_GPA20	0	non-KB BL	RH159
	1	KB BL	RH153
PCH_GPA17	0	Reserved	RH847
	1	Reserved	RH846
PCH_GPH19	0	Reserved	RH849
	1	Reserved	RH848
PCH_GPH21	0	Reserved	RH851
	1	Reserved	RH852

DRAM	Memory Down(DDR4)		DRAMCFG	PCH_GPA23	PCH_GPA22	PCH_GPA21
	Samsung 8Gb 2666 MT/s		0(0x000)	L/RH775	L/RH777	L/RH195
8Gb	Hynix 8Gb 2666 MT/s		1(0x001)	L/RH775	L/RH777	H/RH163
	Micron 8Gb 2666 MT/s		2(0x010)	L/RH775	H/RH776	L/RH195
	Samsung 4Gb 2400 MT/s		3(0x011)	L/RH775	H/RH776	H/RH163
8Gb	Hynix 4Gb 2400 MT/s		4(0x100)	H/RH774	L/RH777	L/RH195
	Micron 4Gb 2400 MT/s		5(0x101)	H/RH774	L/RH777	H/RH163
	X		6(0x110)	H/RH774	H/RH776	L/RH195
	SO-DIMM		7(0x111)	H/RH774	H/RH776	H/RH163

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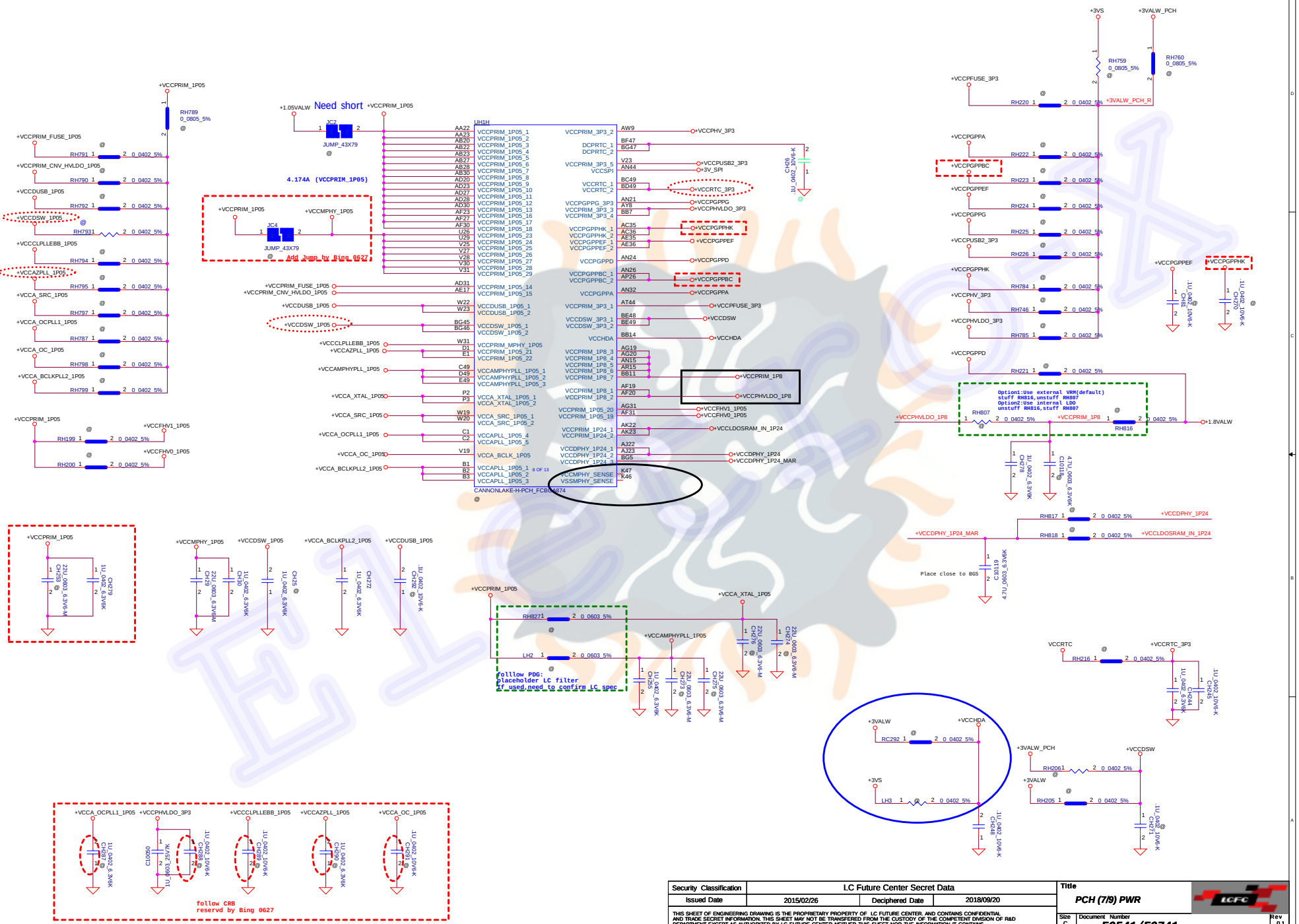
Title: PCH (6/9) GPPPABCD, I2C

Size: C | Document Number: FG541/FG741 | Rev: 0.1

Date: Thursday, January 03, 2019 | Sheet 20 of 69

Eletro-X



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Issued Date	2015/02/26	Deciphered Date	2018/09/20

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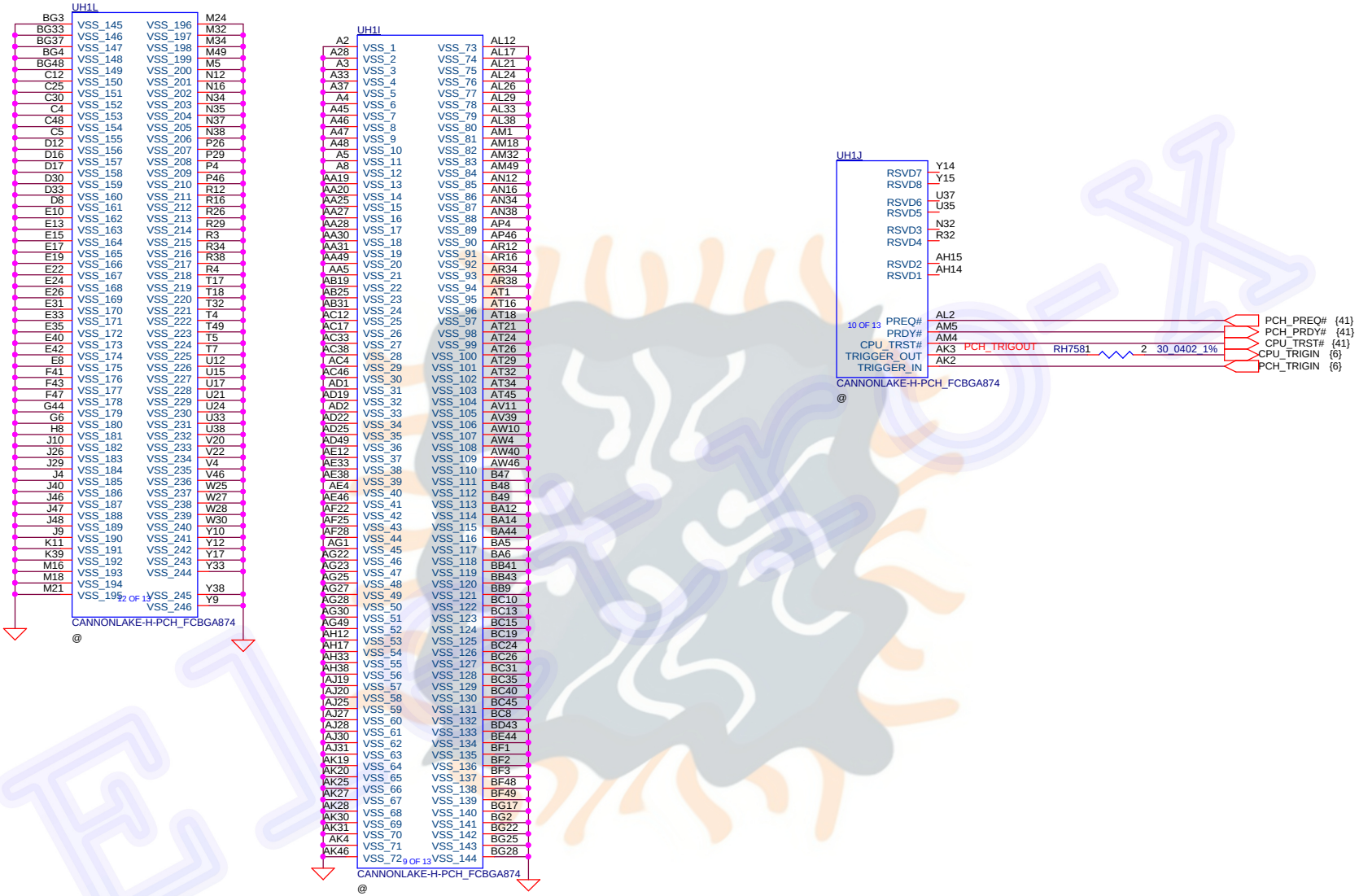
Title: PCH (7/9) PWR

Size: C | Document Number: FG541/FG741 | Rev: 0.1

Date: Tuesday, February 26, 2019 | Sheet 21 of 69

Eletro-X



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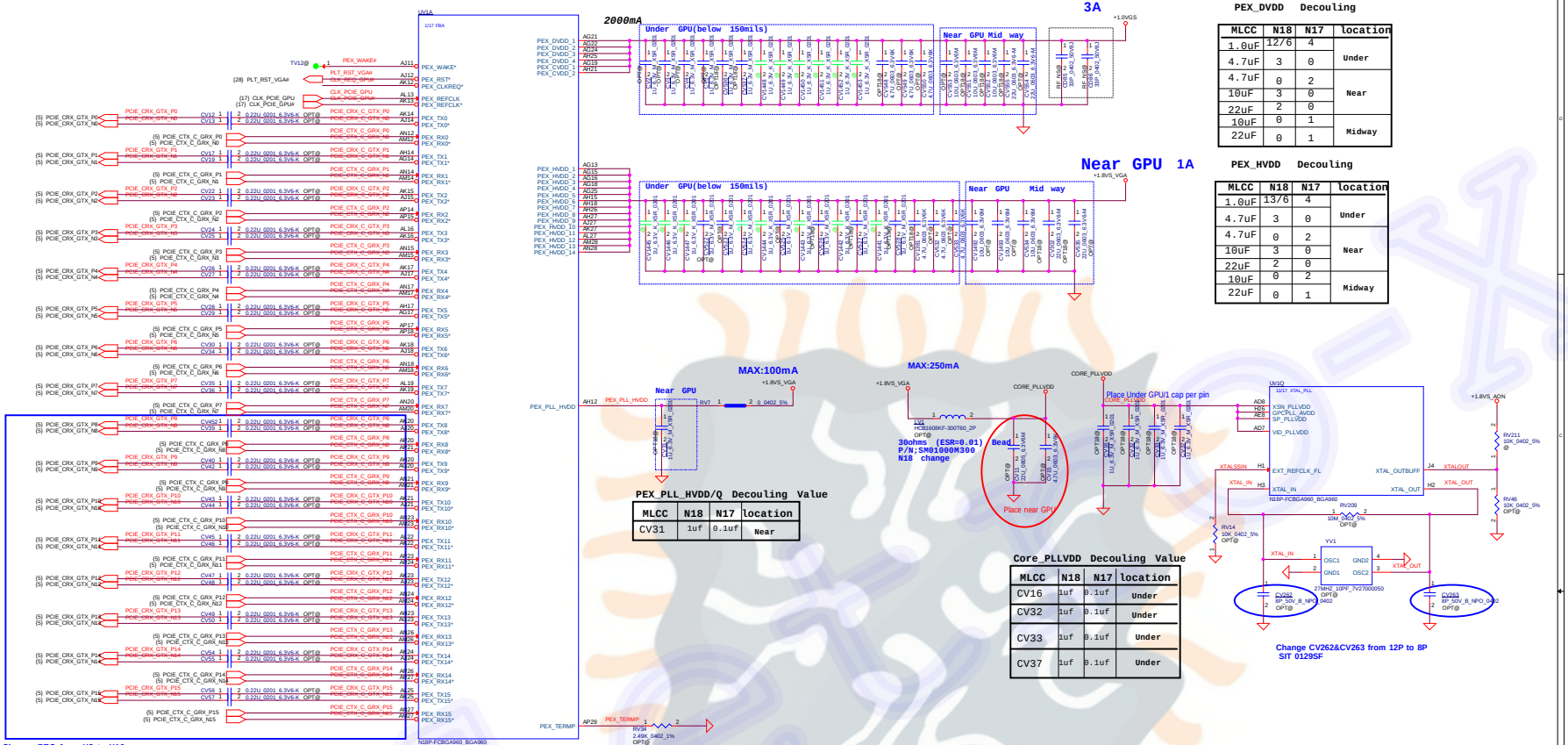
Title

PCH (9/9) VSS

Size	Document Number	Rev
B	FG541/FG741	0.1

Date: Thursday, January 03, 2019 Sheet 22 of 69

Eletro-X



PEX_DVDD Decouling

MLCC	N18	N17	location
1.0uF	12/6	4	Under
4.7uF	3	0	
4.7uF	0	2	Near
10uF	3	0	
22uF	2	0	
10uF	0	1	Midway
22uF	0	1	

PEX_HVDD Decouling

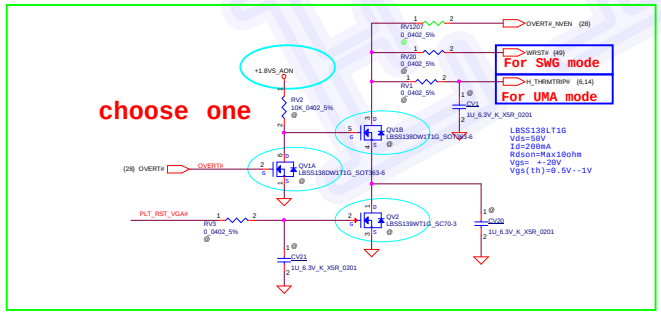
MLCC	N18	N17	location
1.0uF	13/6	4	Under
4.7uF	3	0	
4.7uF	0	2	Near
10uF	3	0	
22uF	2	0	
10uF	0	2	Midway
22uF	0	1	

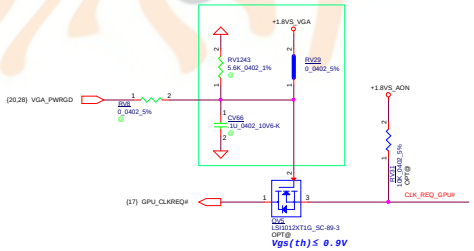
PEX_PLL_HVDD/Q Decouling Value

MLCC	N18	N17	location
CV31	1uf	0.1uf	Near

Core_PLLVDD Decouling Value

MLCC	N18	N17	location
CV16	1uf	0.1uf	Under
CV32	1uf	0.1uf	Under
CV33	1uf	0.1uf	Under
CV37	1uf	0.1uf	Under





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Title: N17P_(1/6):PEG I/F

Size: A3 | Document Number: FG541/FG741 | Rev: 0.1

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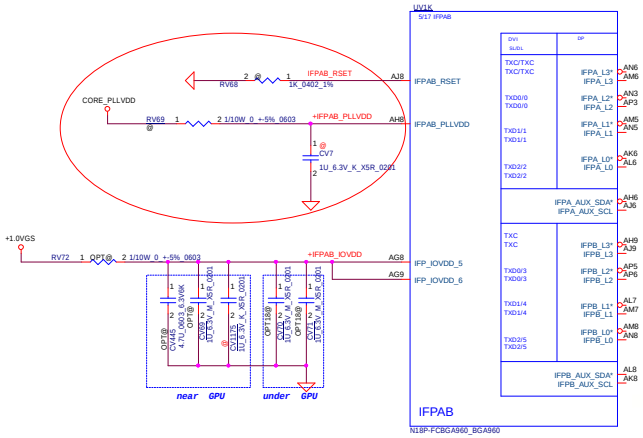
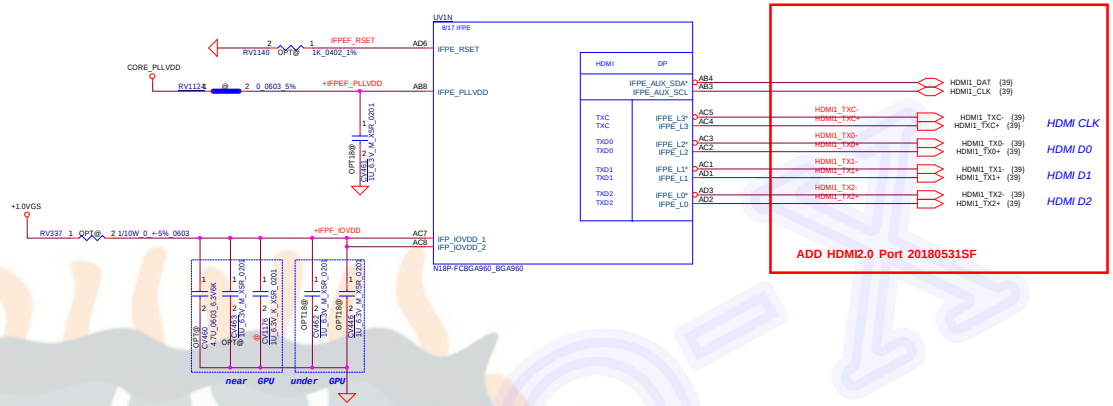
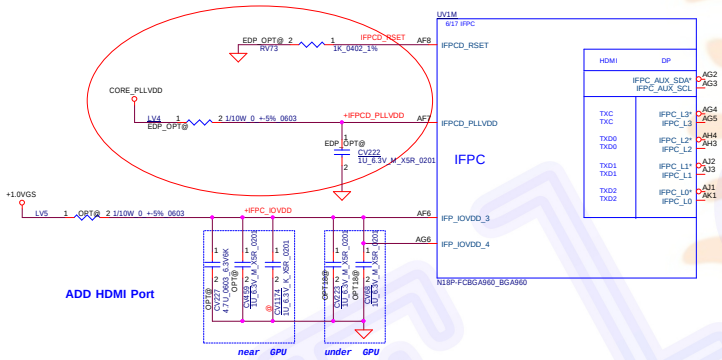
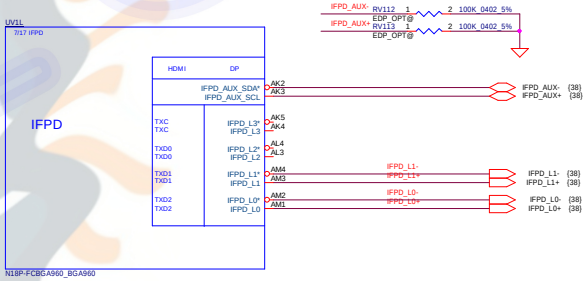
Eletro-X

Ref NV DG-08780-001
If an IFP link is unused, in general it should be left unconnected.
This includes Main and Aux links.
IFPxy_RSET and IFPxy_PLLVDD (xy=AB,CD,EF)
can be left unconnected if neither of IFPx /IFPy is in use









Decouling Value

MLCC	N18	N17	location
CV7	1uf	0.1uf	Under
CV222	1uf	0.1uf	Under
CV461	1uf	0.1uf	Under
CV70	1uf	0.1uf	Under
CV71	1uf	0.1uf	Under
CV223	1uf	0.1uf	Under
CV68	1uf	0.1uf	Under
CV462	1uf	0.1uf	Under
CV484	1uf	0.1uf	Under

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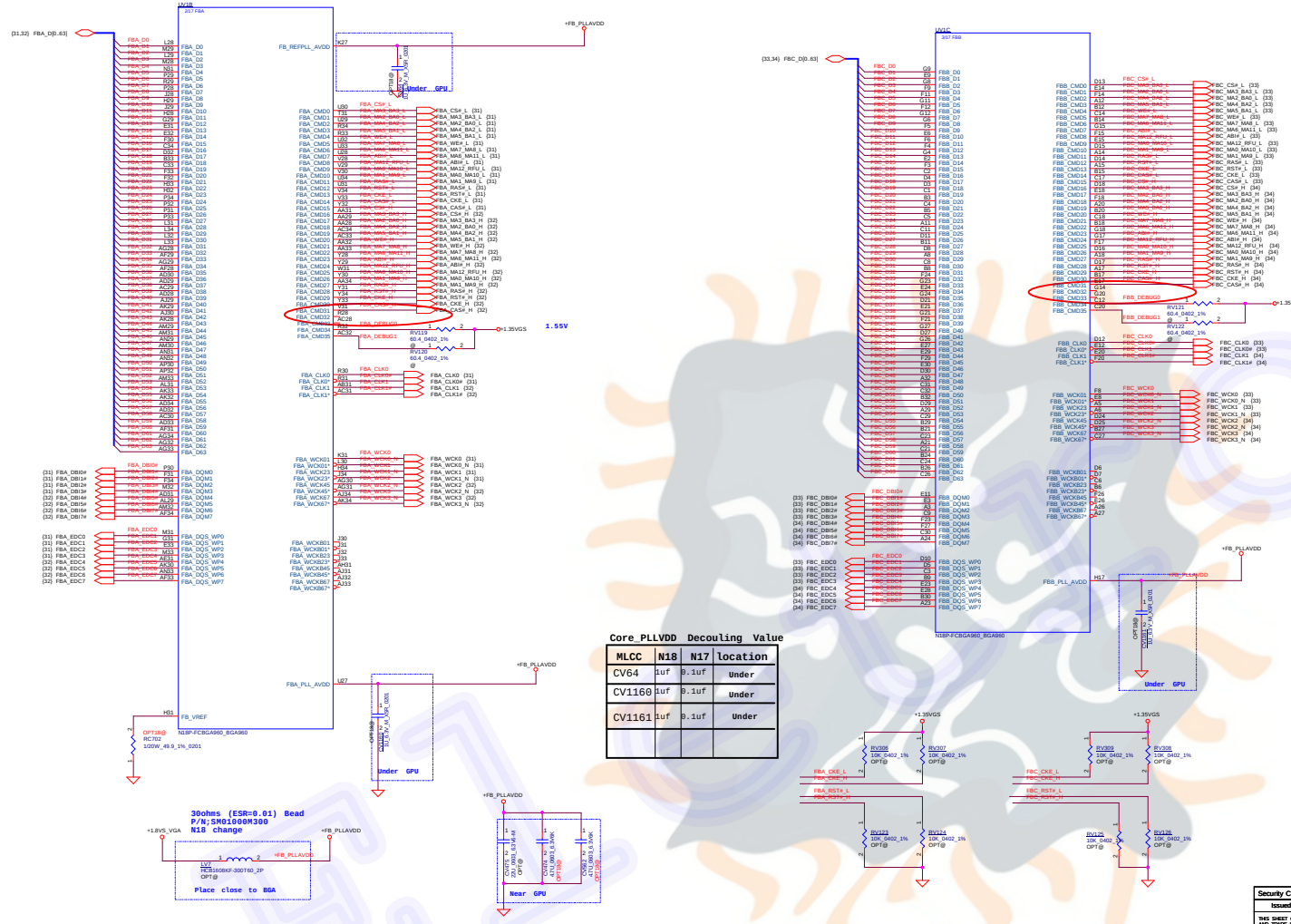
Title: N17P_(2/6):DIGITAL OUT I/F

Size: Custom | Document Number: FG541/FG741 | Rev: 0.1

Date: Wednesday, February 27, 2019 | Sheet 26 of 69

Eletro-X



Core_PLLVDD Decouling Value

MLCC	N18	N17	location
CV64	1uf	0.1uf	Under
CV1160	1uf	0.1uf	Under
CV1161	1uf	0.1uf	Under

GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/20	Deciphered Date	2018/09/20

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Title: N17P_(3/6):VRAM I/F

Size: | Document Number: FG541/FG741 | Rev: 0.1

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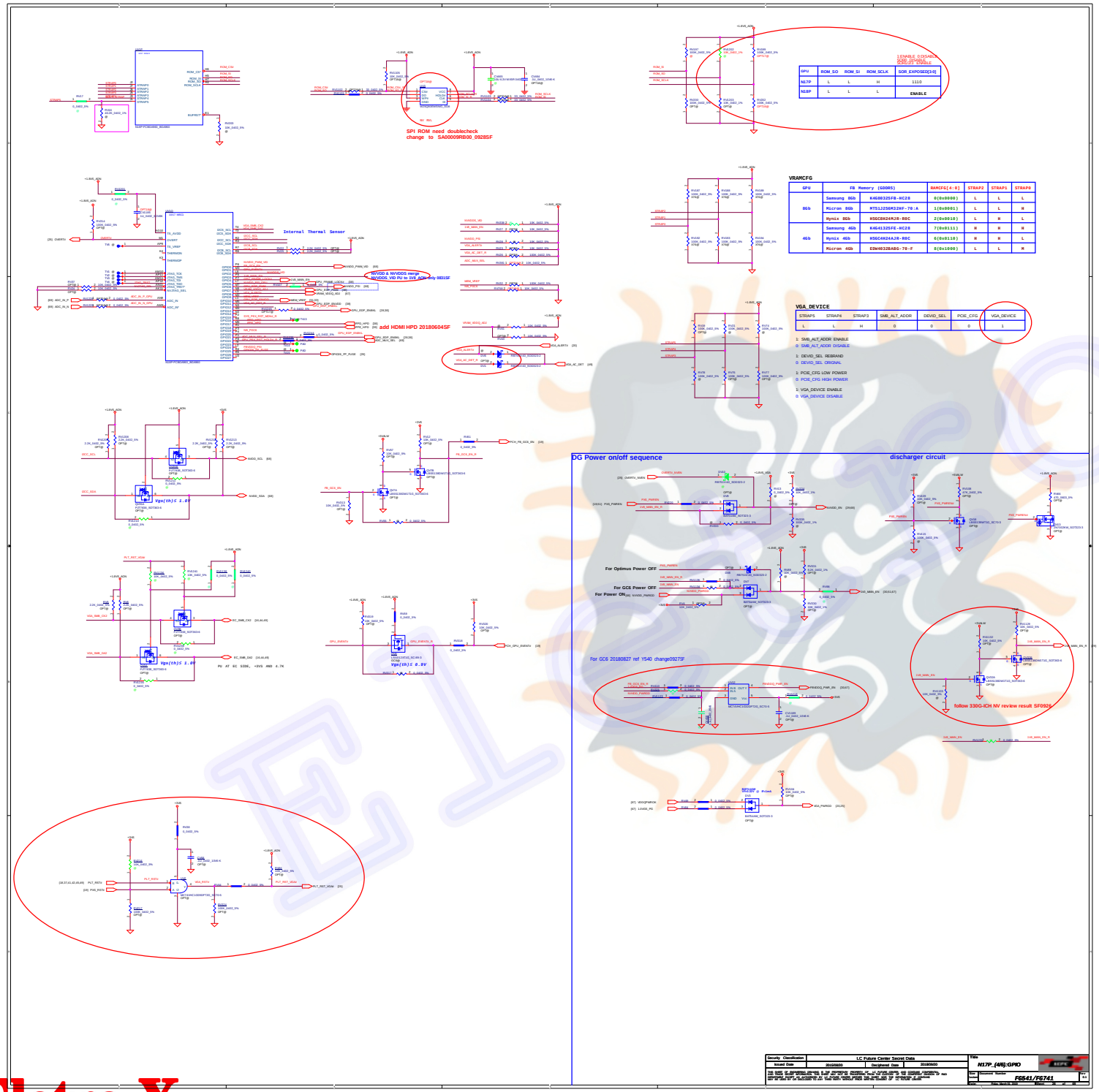
Eletro-X



GPU	ROM_SO	ROM_SI	ROM_SCLK	SOM_EXPOSED[3:0]
N17P	L	L	H	1110
N18P	L	L	L	ENABLE

1:ENABLE 0:DISABLE
SOM DISABLE
SOM_EN ENABLE

VRAMCFG

GPU	FB Memory (GDDR5)		VARCFG[4:0]	STRAP2	STRAP1	STRAP0
8Gb	Samsung 8Gb	K4G80325FB-HC28	0(0x0000)	L	L	L
	Micron 8Gb	MT51J256M32HF-70:A	1(0x0001)	L	L	H
	Hynix 8Gb	H5GC8H24MJR-R0C	2(0x0010)	L	H	L
4Gb	Samsung 4Gb	K4G41325FE-HC28	7(0x0111)	H	H	H
	Hynix 4Gb	H5GC4H24AJR-R0C	6(0x0110)	H	H	L
	Micron 4Gb	EDW4032BABG-70-F	8(0x1000)	L	L	H

VGA_DEVICE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	H	0	0	0	1

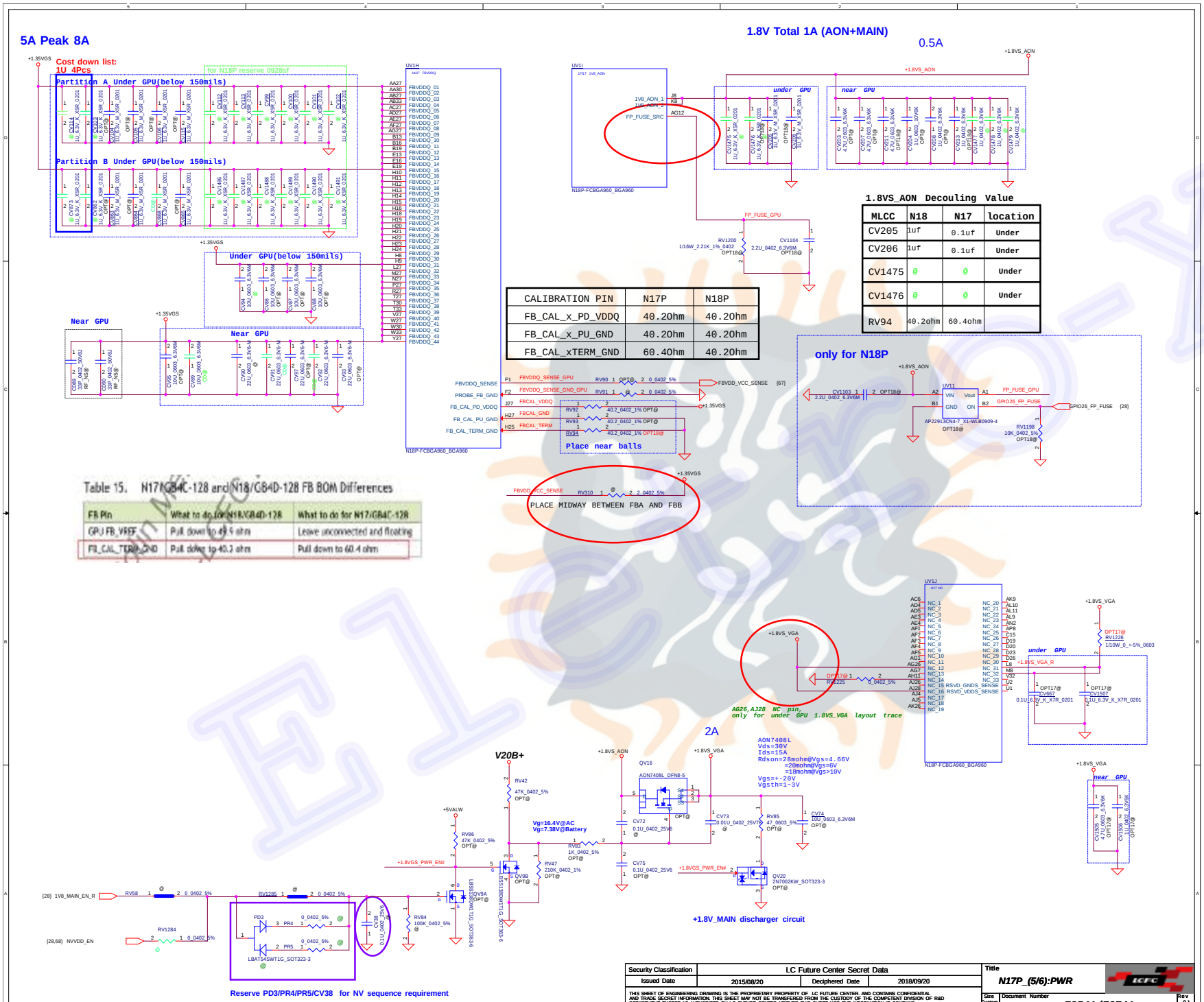
1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE

1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGNAL

1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER

1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE

Eletro-X



CALIBRATION PIN	N17P	N18P
FB_CAL_x_PD_VDDQ	40.2ohm	40.2ohm
FB_CAL_x_PU_GND	40.2ohm	40.2ohm
FB_CAL_xTERM_GND	60.4ohm	40.2ohm

MLCC	N18	N17	location
CV205	1uf	0.1uf	Under
CV206	1uf	0.1uf	Under
CV1475	@	@	Under
CV1476	@	@	Under
RV94	40.2ohm	60.4ohm	

Table 15. N17/GB4C-128 and N18/GB4D-128 FB BOM Differences

FB Pin	What to do for N18/GB4D-128	What to do for N17/GB4C-128
GPU FB_VREF	Pull down to 49.9 ohm	Leave unconnected and floating
FB_CAL_TERM_GND	Pull down to 40.2 ohm	Pull down to 60.4 ohm

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

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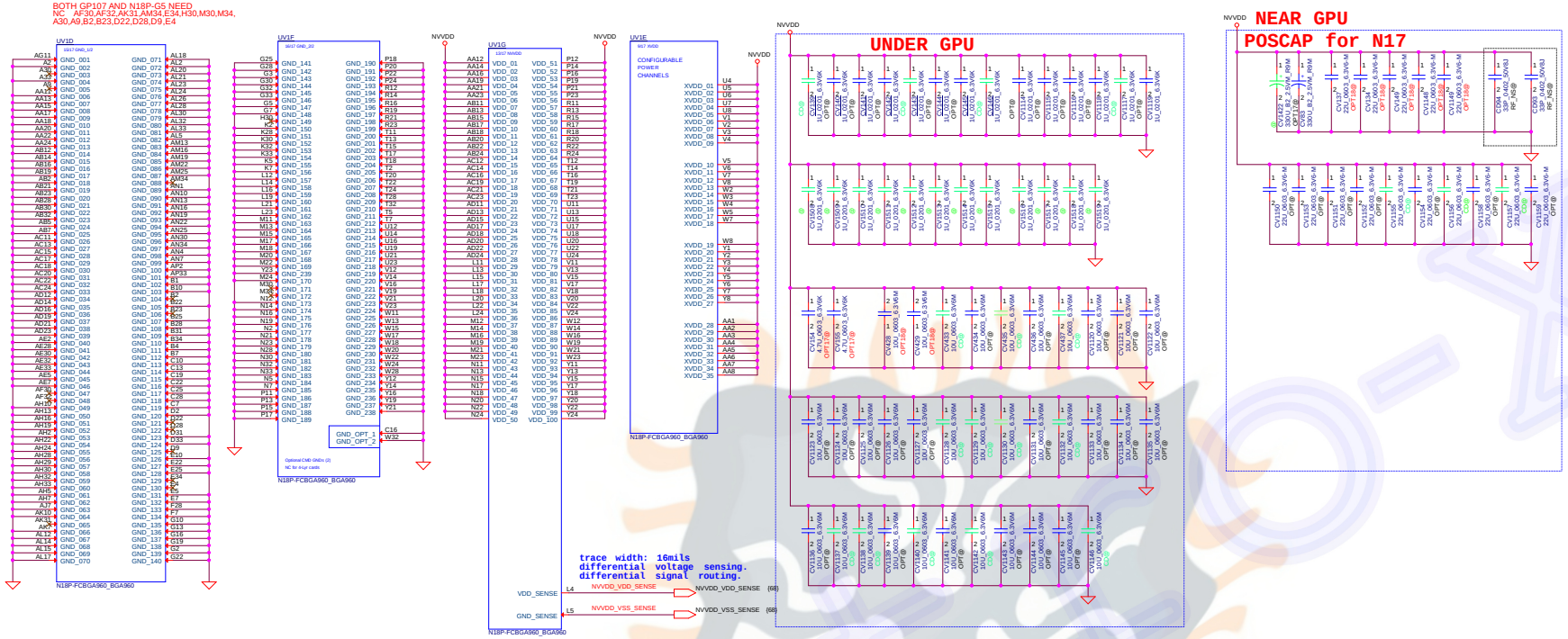
Title: N17P_(5/6):PWR

Size: Custom | Document Number: FG541/FG741 | Rev: 0.1

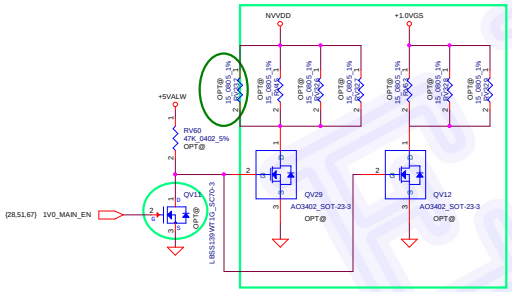
Date: Wednesday, February 27, 2019 | Sheet 29 of 69

Eletro-X

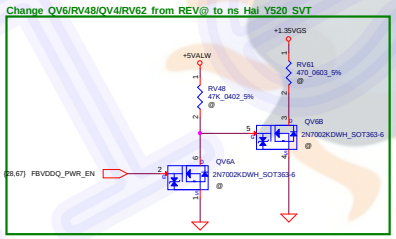


Add RV332 for NVVDDS discharge Hai Y520 SVT

Change NVVDDS & +1.0VGS discharge circuit
HLZ SIV 0725



Change QV6/RV48/QV4/RV62 from REV@ to ns Hai Y520 SVT



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Issued Date	2015/08/20	Deciphered Date	2018/09/20

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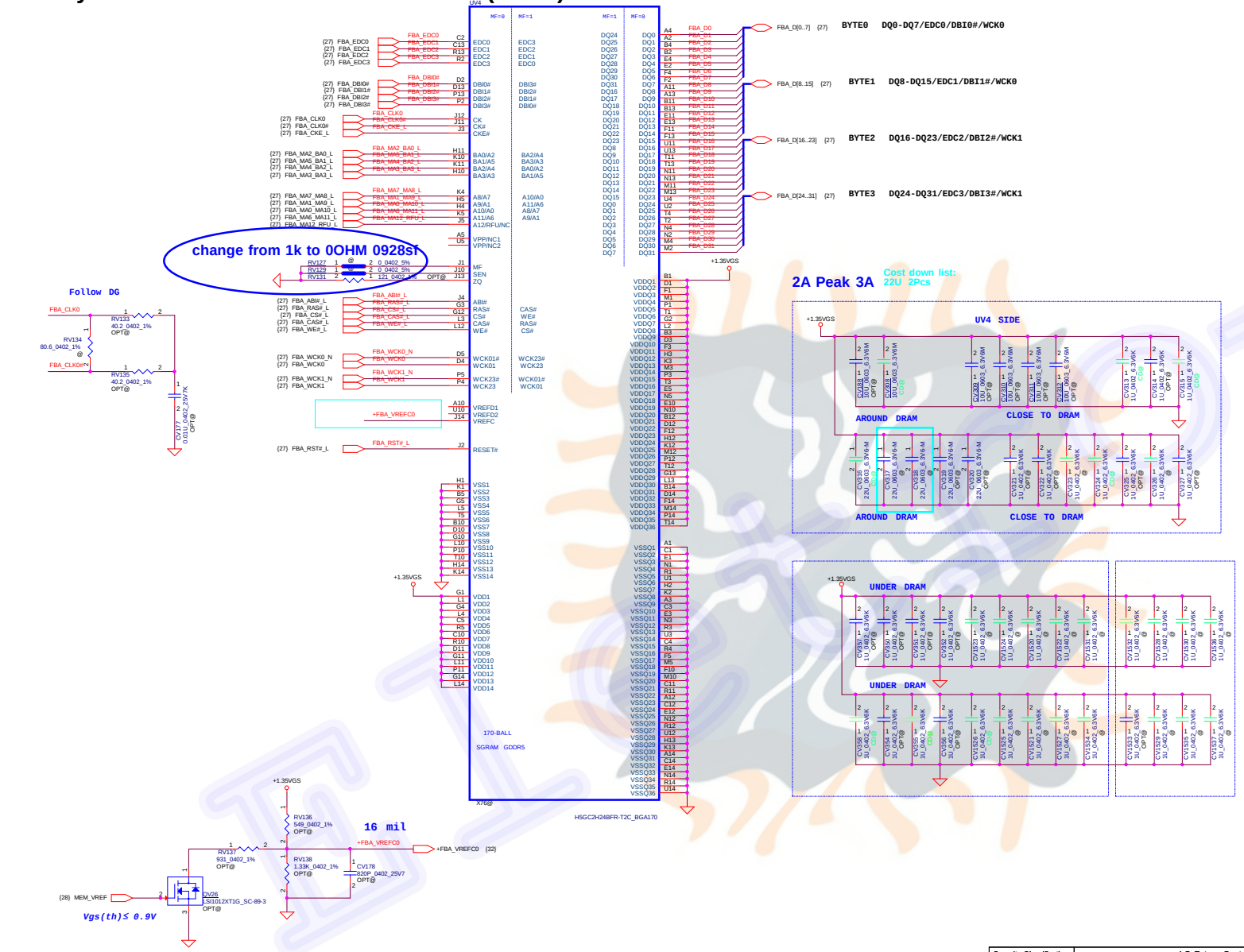
Title: N17P_(6/6):PWR,VSS

Size: Custom | Document Number: FG541/FG741 | Rev: 0.1

Date: Tuesday, January 22, 2019 | Sheet 30 of 69

Eletro-X

Memory Partition A - Lower 64 bits(MF=0)



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

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Title: N17P_GDDR5_A Lower

Size: Custom | Document Number: FG541/FG741 | Rev: 0.1

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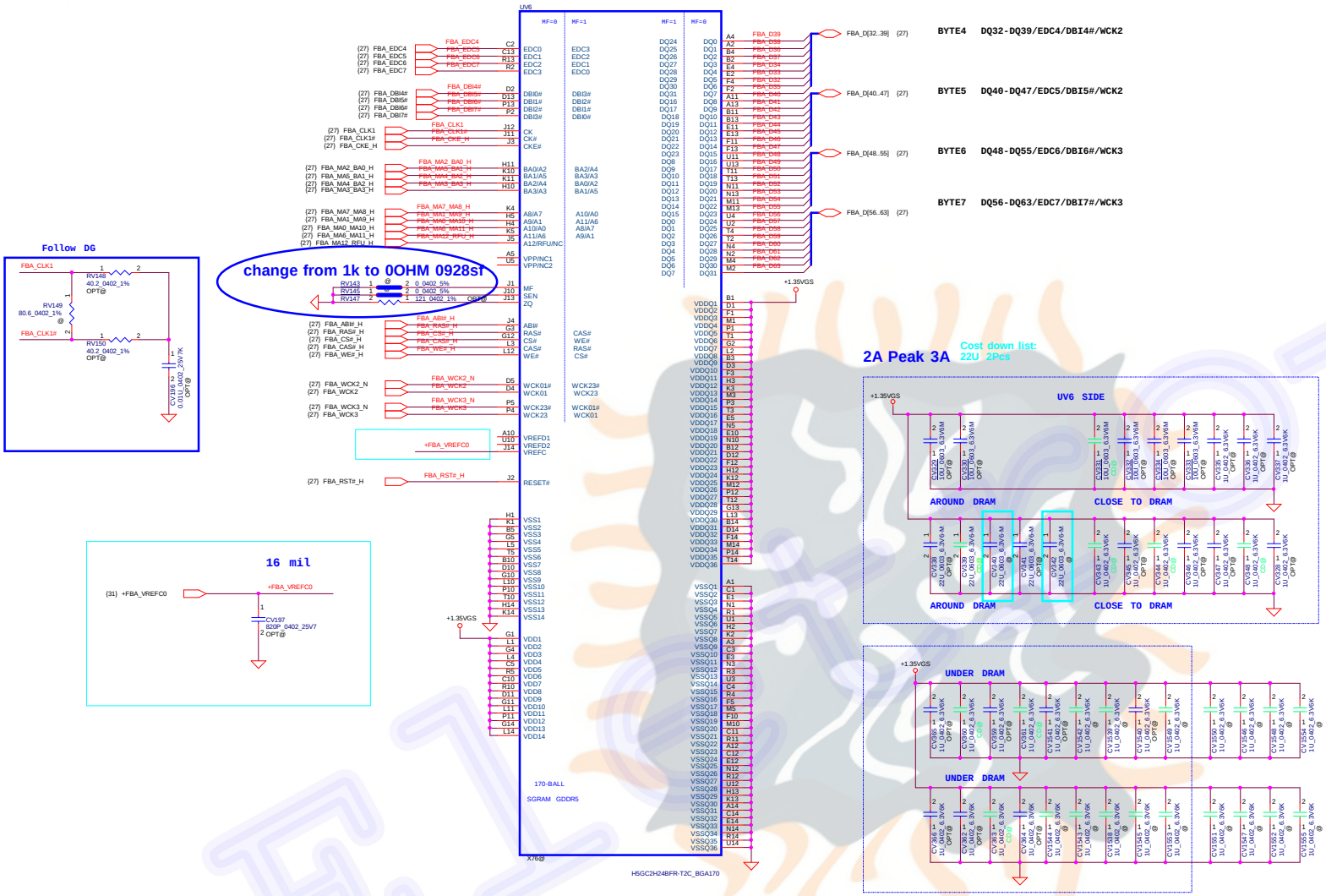
Eletro-X

Memory Partition A- Upper 64 bits(MF=0)



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

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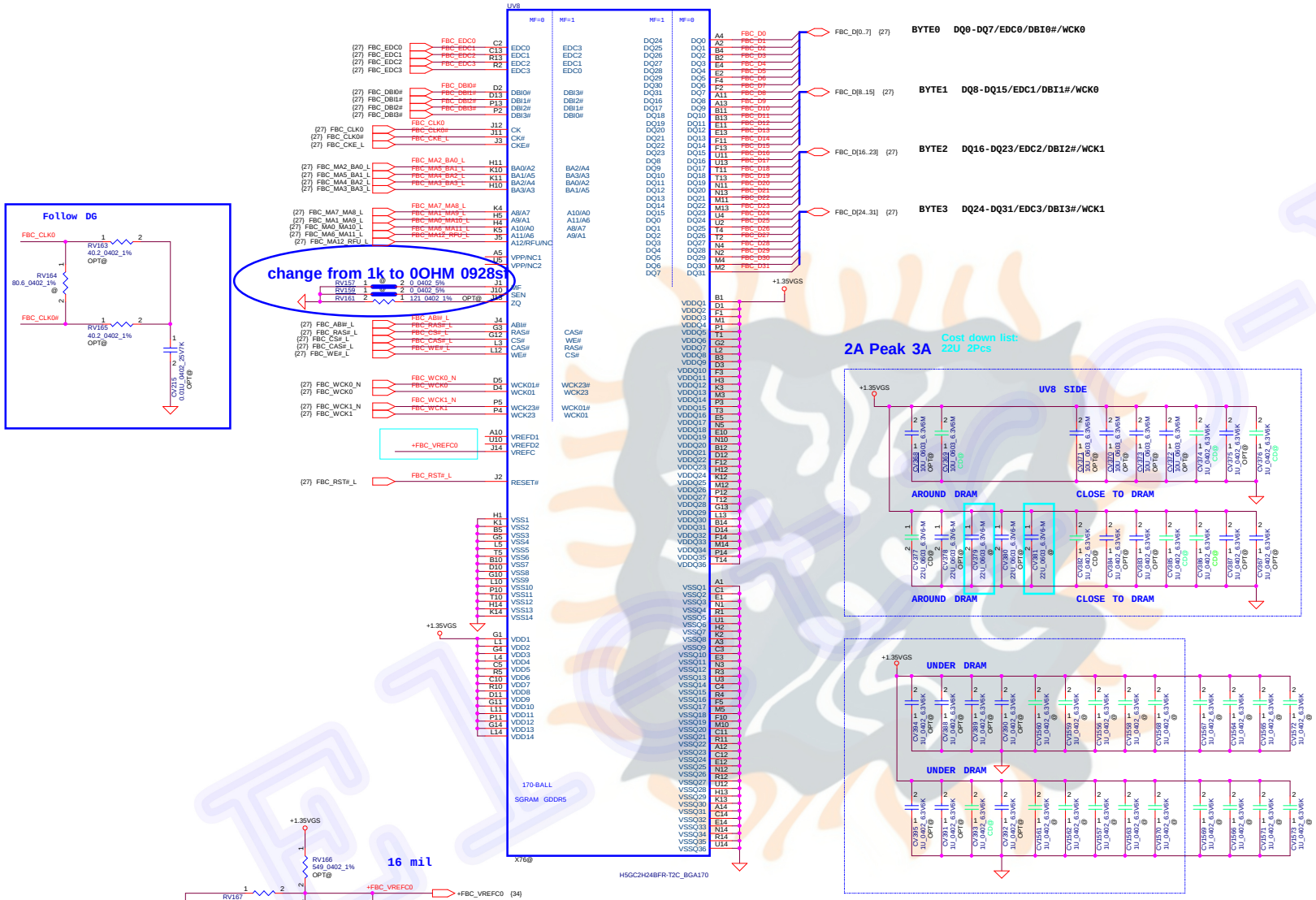
Title: N17P_GDDR5_A Upper

Size: Custom | Document Number: FG541/FG741 | Rev: 0.1

Date: Tuesday, February 26, 2019 | Sheet 32 of 69

Eletro-X

Memory Partition B - Lower 32 bits(MF=0)



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

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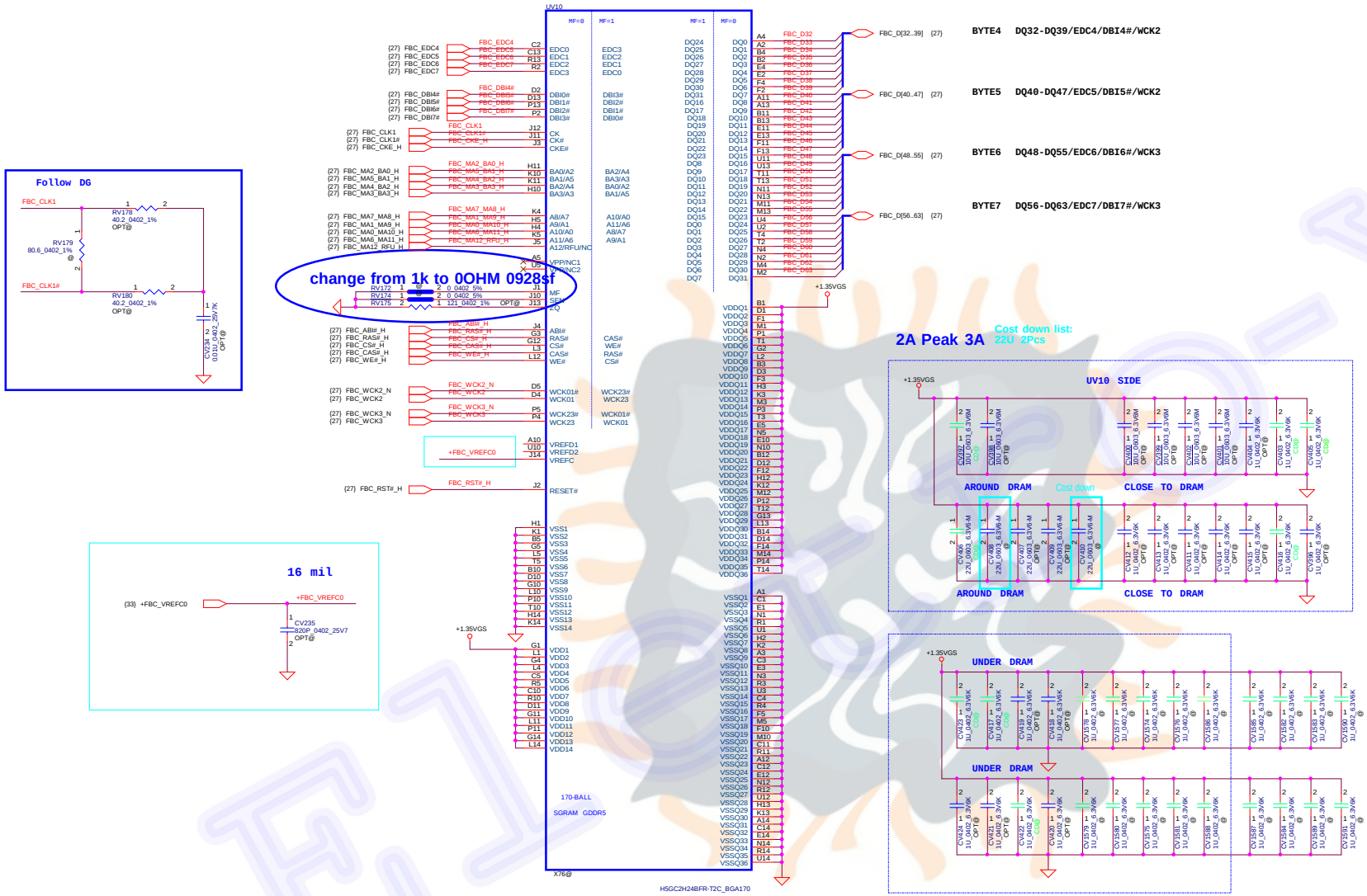
Title: N17P_GDDR5_B Lower

Size: Custom | Document Number: FG541/FG741 | Rev: 0.1

Date: Tuesday, February 26, 2019 | Sheet 33 of 69

Eletro-X

Memory Partition B - Upper 32 bits(MF=0)



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

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Title: N17P_GDDR5_B Upper

Size: Custom | Document Number: FG541/FG741 | Rev: 0.1

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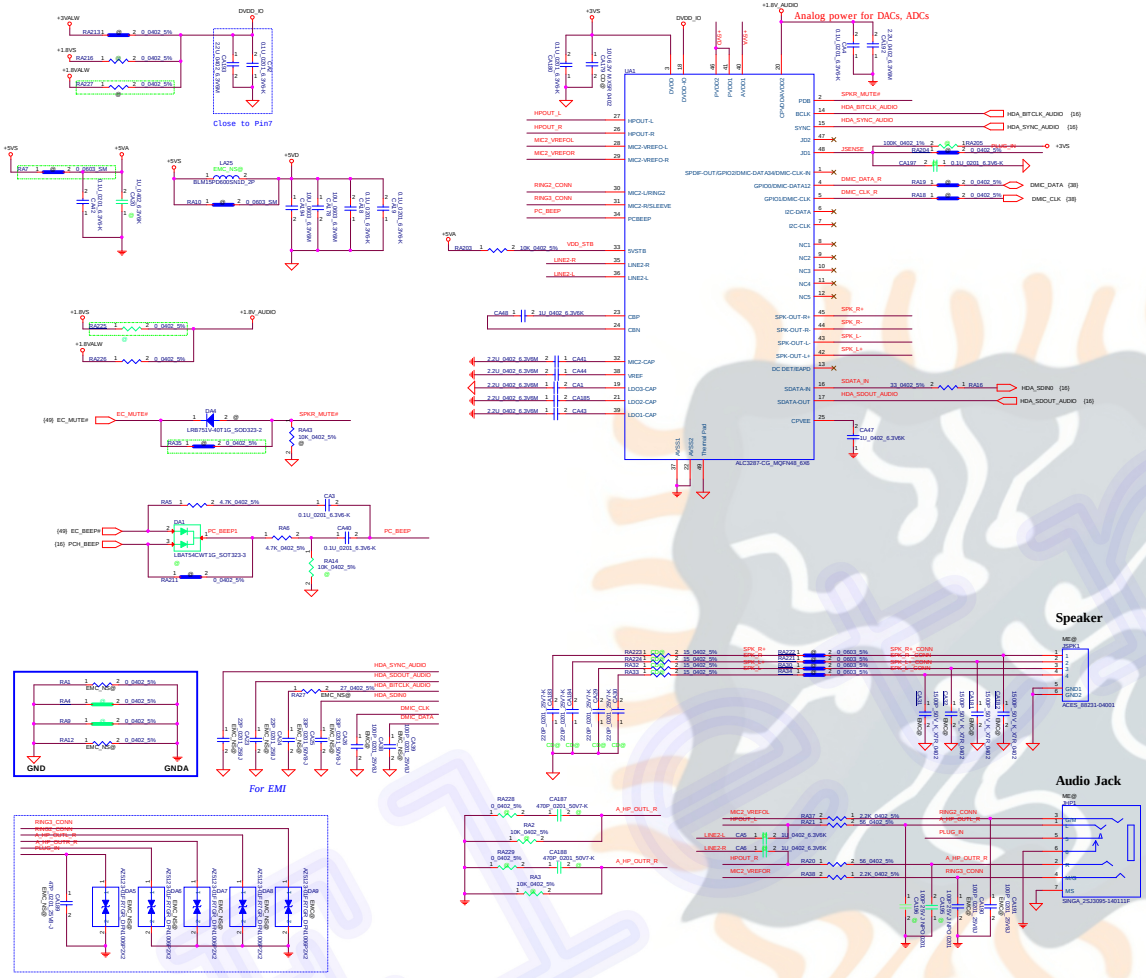
Eletro-X



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2015/09/20

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Title: Codec & CR_RTS5199

Size: D | Document Number: F6541/F6741 | Rev: 0.1

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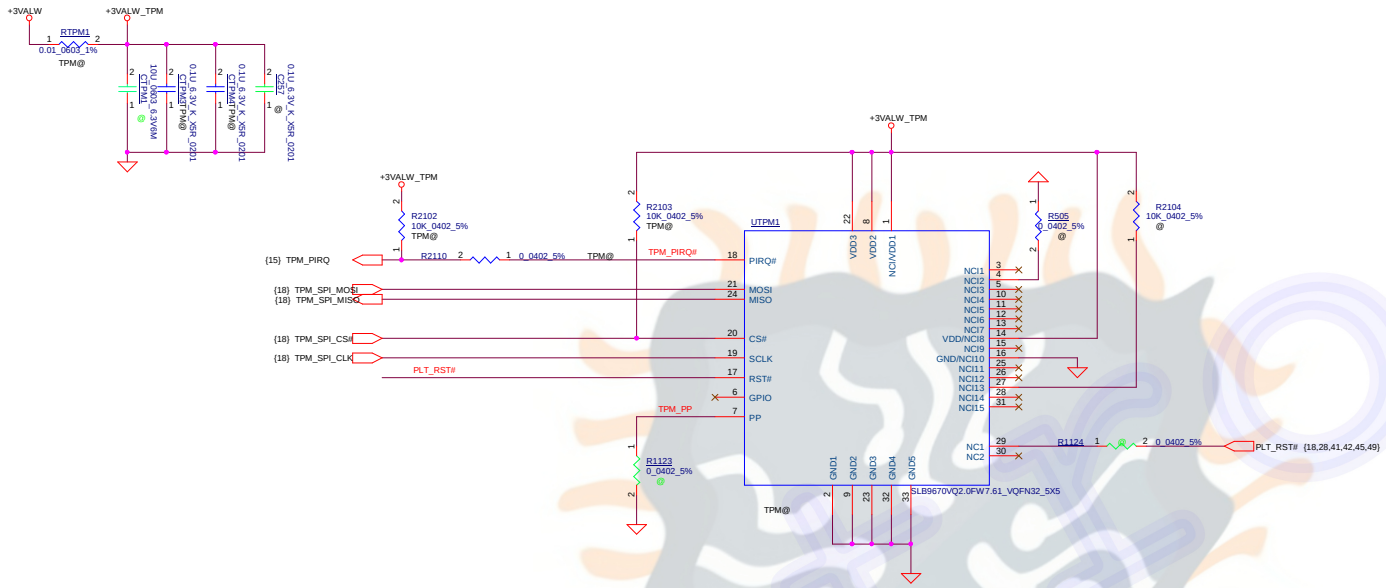
Eletro-X



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

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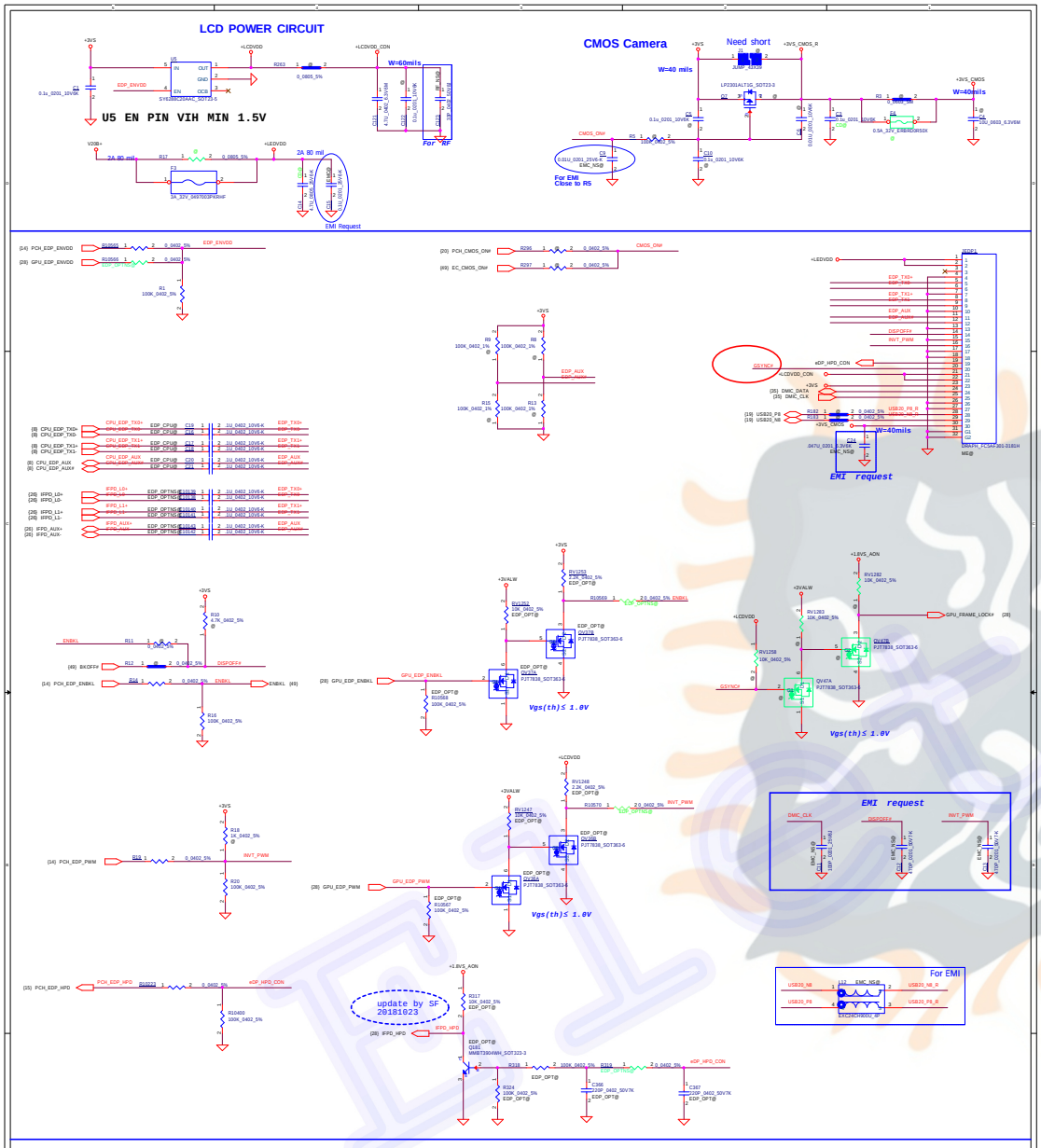
Title: **TPM**

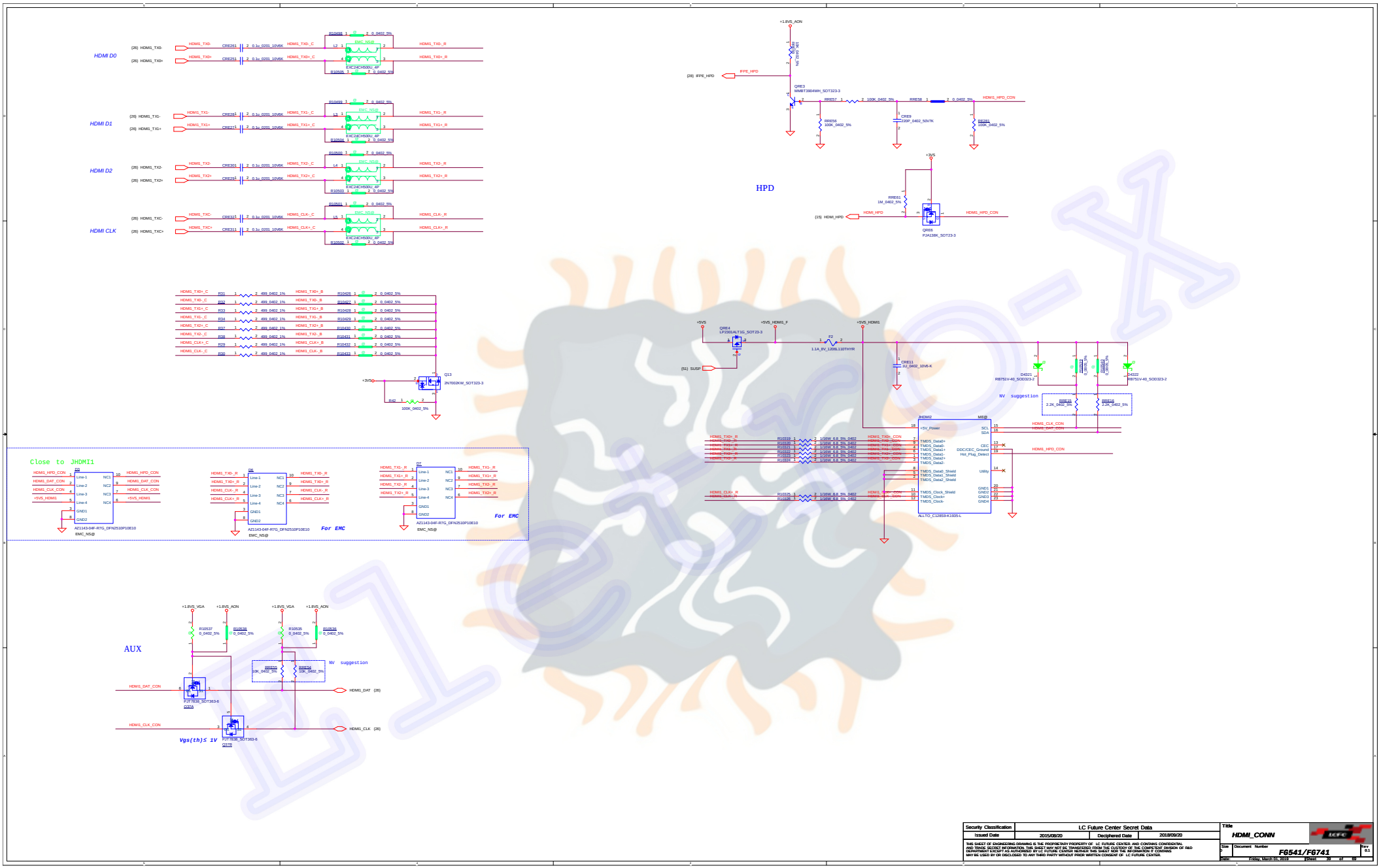
Size: C | Document Number: **FG541/FG741** | Rev: 0.1

Date: Thursday, January 03, 2019 | Sheet 37 of 69

Eletro-X


LCD POWER CIRCUIT
U5 EN PIN VIH MIN 1.5V
W=60mils
For RF
CMOS Camera
Need short
W=40 mils
W=40mils
For EMI Close to R5
2A 80 mil
EMI Request
EMI request
Vgs(th)≤ 1.0V
update by SF 20181023
For EMI
Touch Screen delete TS function0704SF
Security Classification LC Future Center Secret Data
Issued Date 2015/08/20 Deciphered Date 2018/09/20
Title eDP/CMOS/Touch screen
Size Document Number Rev
F6541/F6741 0.1
Date: Wednesday, February 27, 2019 Sheet 28 of 68

Eletro-X


HDMI D0
HDMI D1
HDMI D2
HDMI CLK
HPD
AUX
Close to JHDMI1
For EMC
NV suggestion
Vgs(th)≤ 1V
Security Classification
LC Future Center Secret Data
Issued Date
2015/08/20
Deciphered Date
2018/09/20
Title
HDMI_CONN
F6541/F6741
Friday, March 01, 2019

Eletro-X

TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

LOGIC

TABLE : PCH ITP DEBUG REPORT

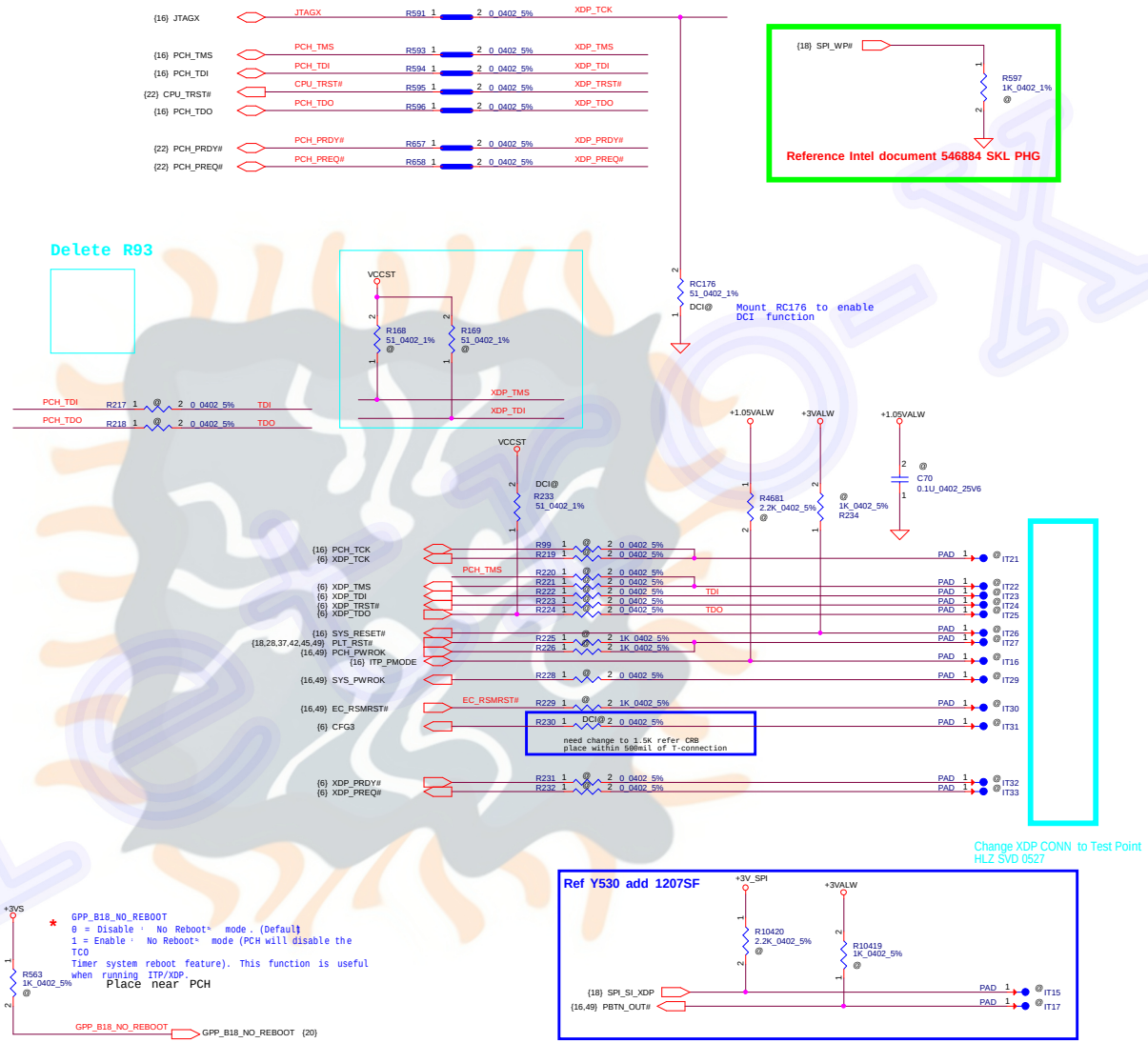
	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

LOGIC

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

LOGIC



Ref Y530 add 1207SF

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

Title: Blank

Size: C | Document Number: FG541/FG741 | Rev: 0.1

Date: Thursday, January 03, 2019 | Sheet 41 of 69

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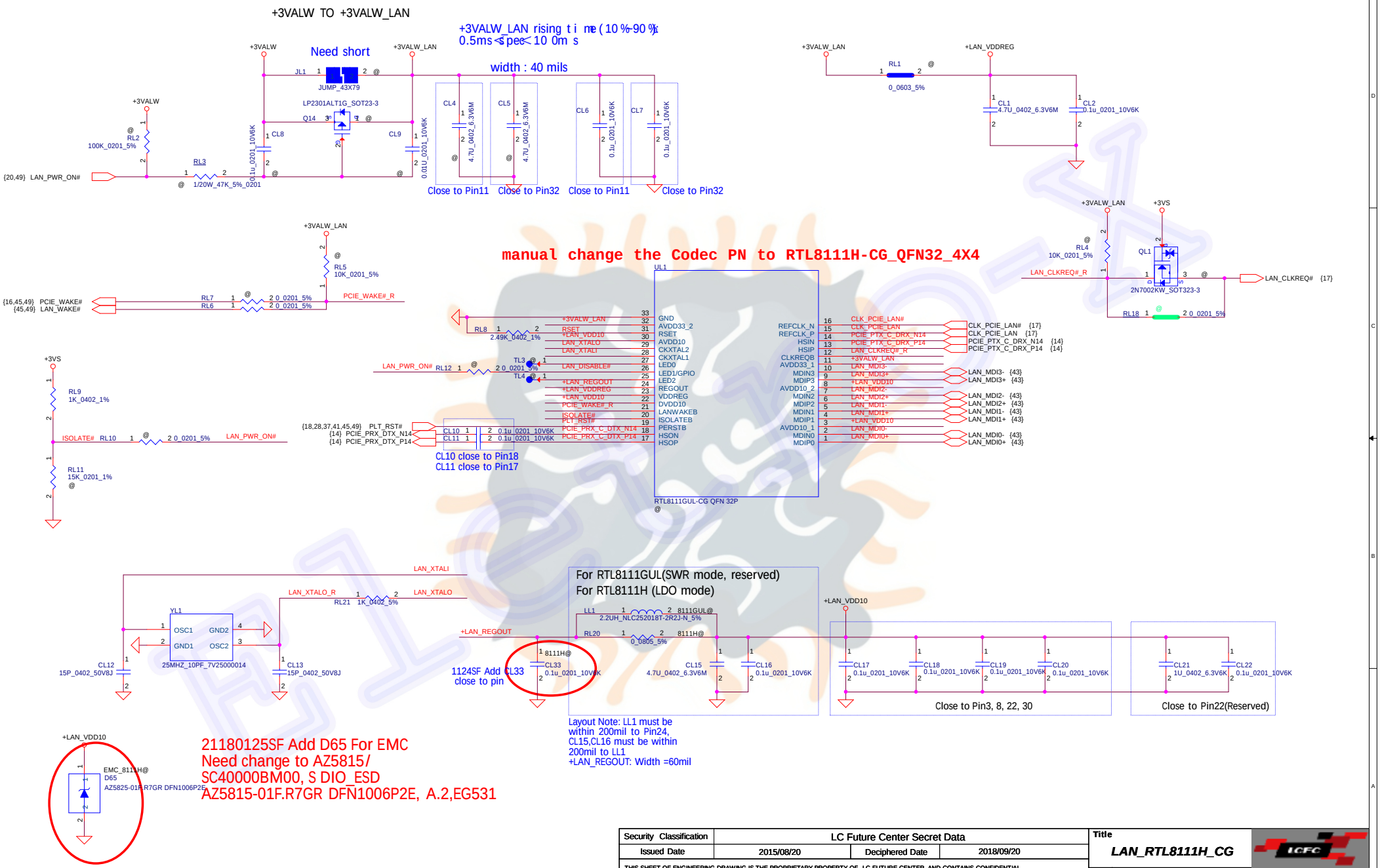
Eletro-X



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

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Title: LAN_RTL8111H_CG

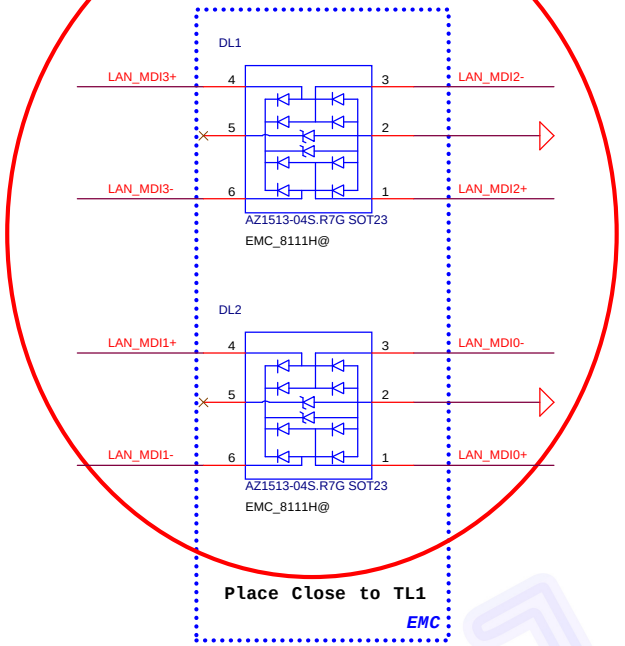
Size: Custom | Document Number: FG541/FG741 | Rev: 0.1

Date: Wednesday, February 27, 2019 | Sheet 42 of 69

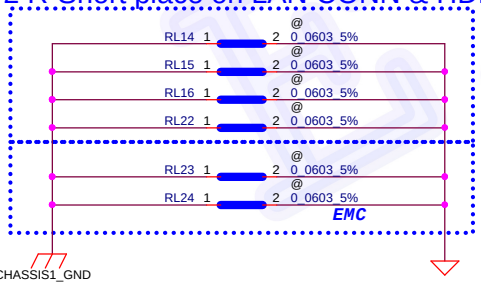
Eletro-X

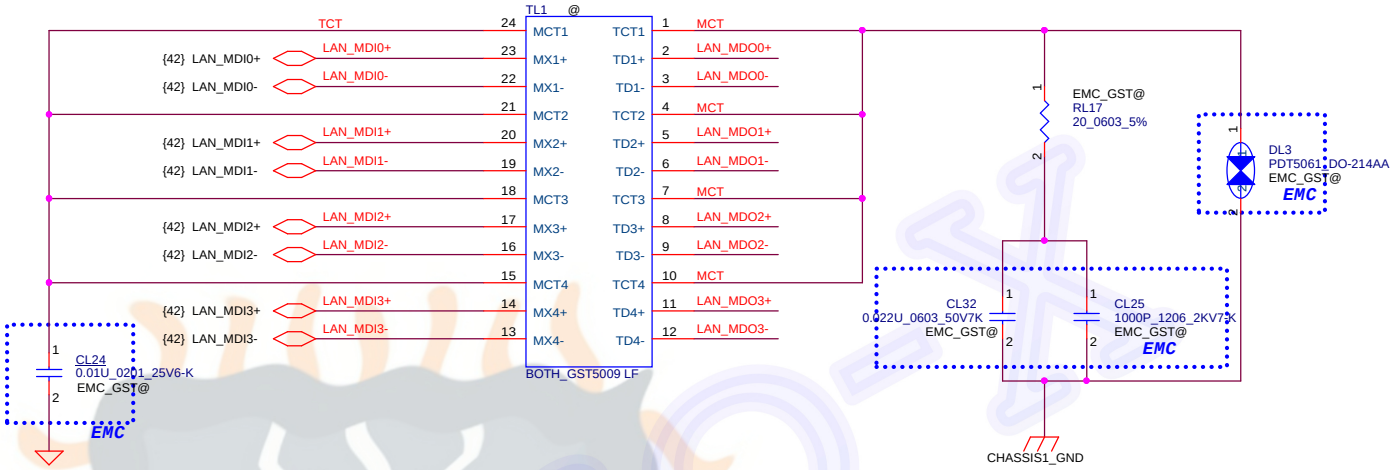
0907SF change DL1/DL2 to
S DIO(BR) AZ1215-04S.R7G SOT23-6L
PN:SC300005900 for 8111H

20180125SF:For EMC debug DL1 & DL2
Need change to SC300006100,
S DIO(BR) AZ1135-04S.R7G SOT23, A.1,EG531

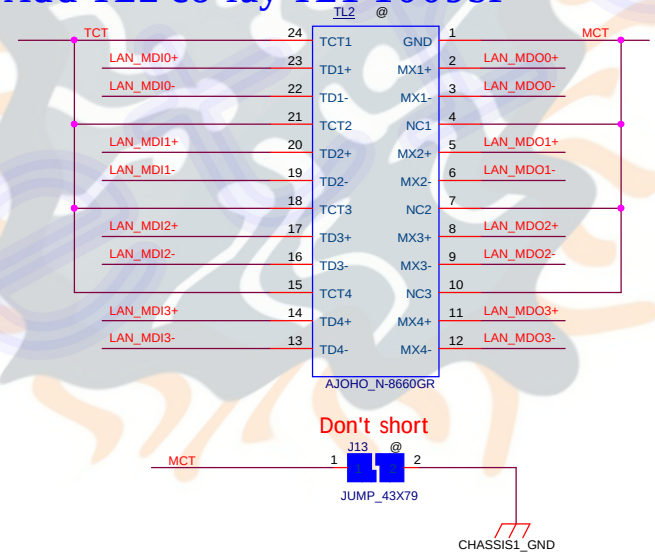


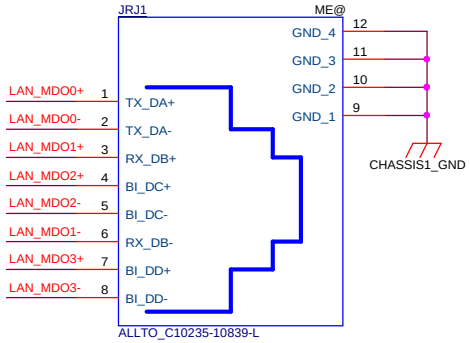
1204SF update,
4 R-Short place on DC-IN CONN & LAN CONN,
2 R-Short place on LAN CONN & HDMI CONN





Add TL2 co-lay TL1 1009SF





8/16 Update RJ45 P/N DC021608091 wei

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

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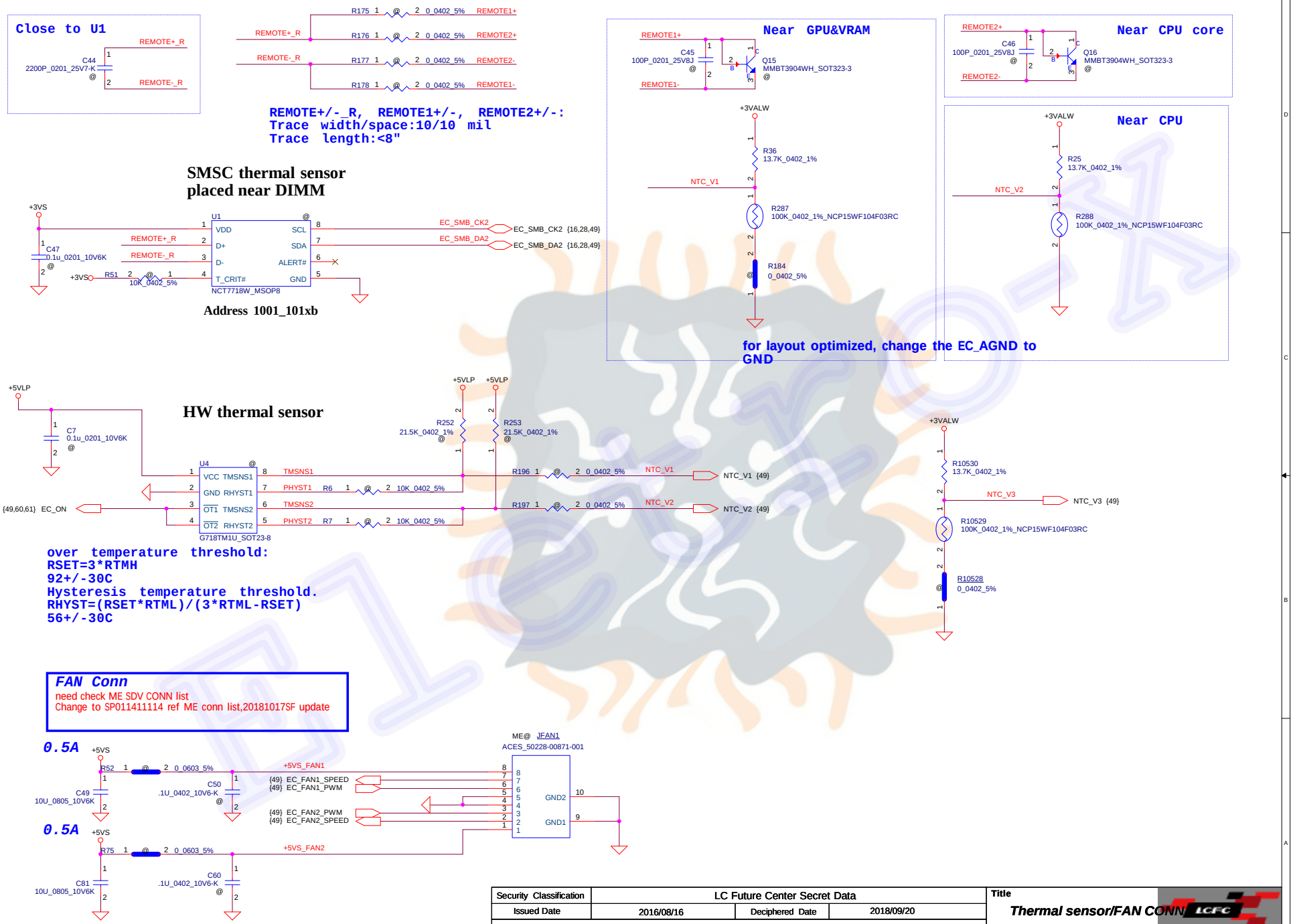
Title: LAN_Transformer

Size: B | Document Number: FG541/FG741 | Rev: 0.1

Date: Saturday, February 02, 2019 | Sheet 43 of 69

Eletro-X



Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2018/09/20

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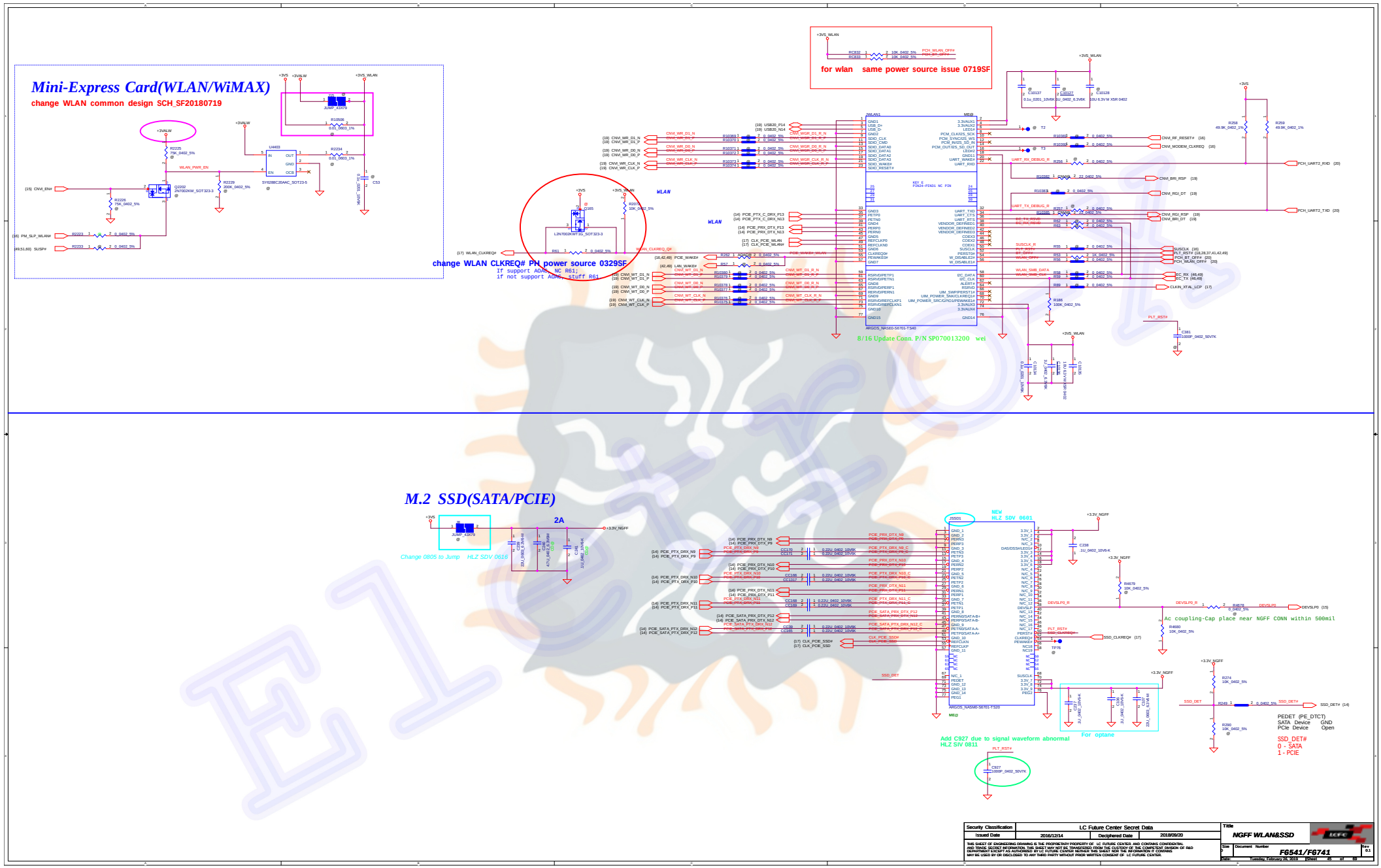
Title: Thermal sensor/FAN CONN

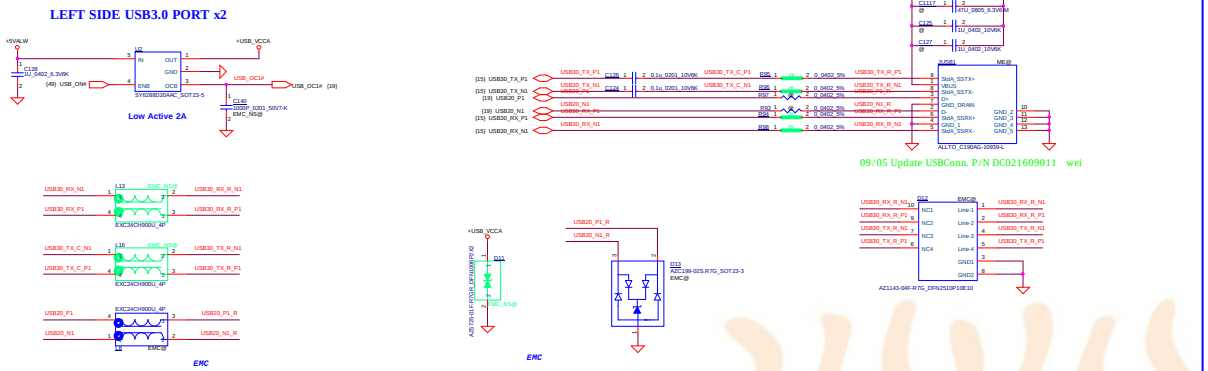
Size: Custom | Document Number: FG541/FG741 | Rev: 0.1

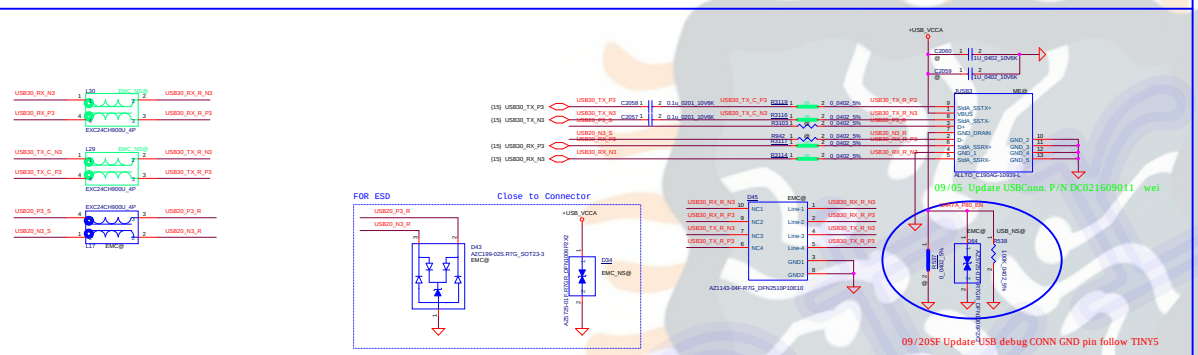
Date: Tuesday, February 26, 2019 | Sheet 44 of 69

Eletro-X


Mini-Express Card(WLAN/WiMAX)
change WLAN common design SCH_SF20180719
for wlan same power source issue 0719SF
WLAN
change WLAN CLKREQ# PH power source 0329SF
If support AOAC NC R61;
if not support AOAC stuff R61
8/16 Update Conn. P/N SP070013200 wei
M.2 SSD(SATA/PCIE)
Change 0805 to Jump HLZ SDV 0616
NEW
HLZ SDV 0601
Ac coupling-Cap place near NGFF CONN within 500mil
Add C927 due to signal waveform abnormal
HLZ SIV 0811
For optane
PEDET (PE_DTCT)
SATA Device GND
PCIe Device Open
SSD_DET#
0 - SATA
1 - PCIE
Security Classification
LC Future Center Secret Data
Issued Date 2016/12/14
Deciphered Date 2018/09/20
Title
NGFF WLAN&SSD
Size D
Document Number
F6541/F6741
Rev 0.1
Date: Tuesday, February 26, 2019
Sheet 26 of 68

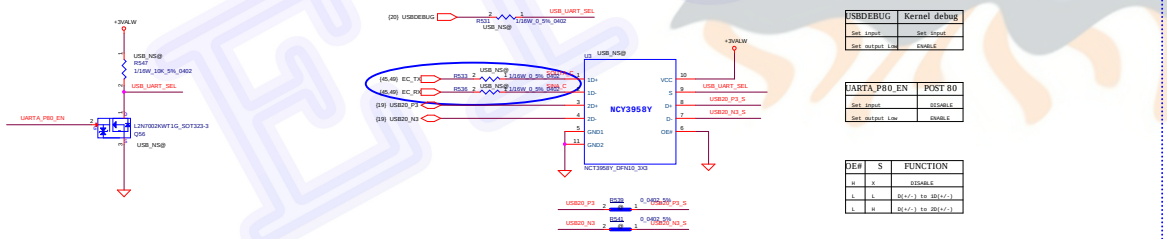
Eletro-X





For USB Debug Function

09/20SF add USB debug follow TINY5
change from SA00007WL0D to SA00007WL00 SF1001
SVT non-staff0322SF



USBDEBUG	Kernel debug
Set input	Set input
Set output Low	ENABLE

UARTA_P80_EN	POST 80
Set input	DISABLE
Set output Low	ENABLE

OE#	S	FUNCTION
H	X	DISABLE
L	L	D(+/-) to 1D(+/-)
L	H	D(+/-) to 2D(+/-)

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

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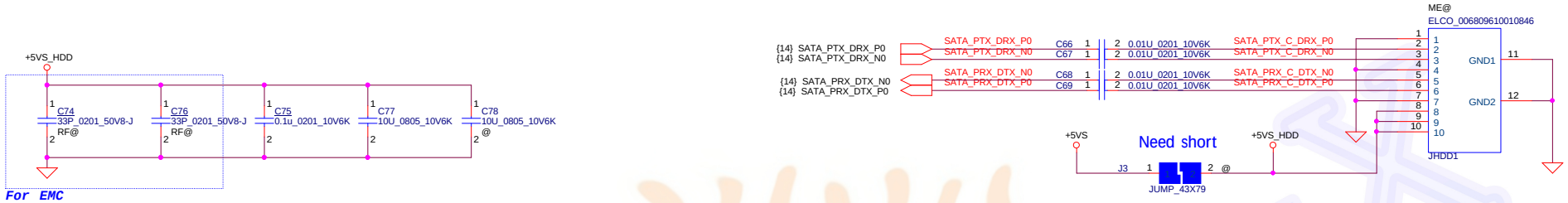
Title: USB3.0 PORT (LEFT)

Size: D | Document Number: F6541/F6741 | Rev: 0.1

Date: Friday, March 01, 2019 | Sheet 46 of 69

SATA HDD Conn.



Delete SATA ODD

8/14 Update SF

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Issued Date	2015/08/20	Deciphered Date	2018/09/20

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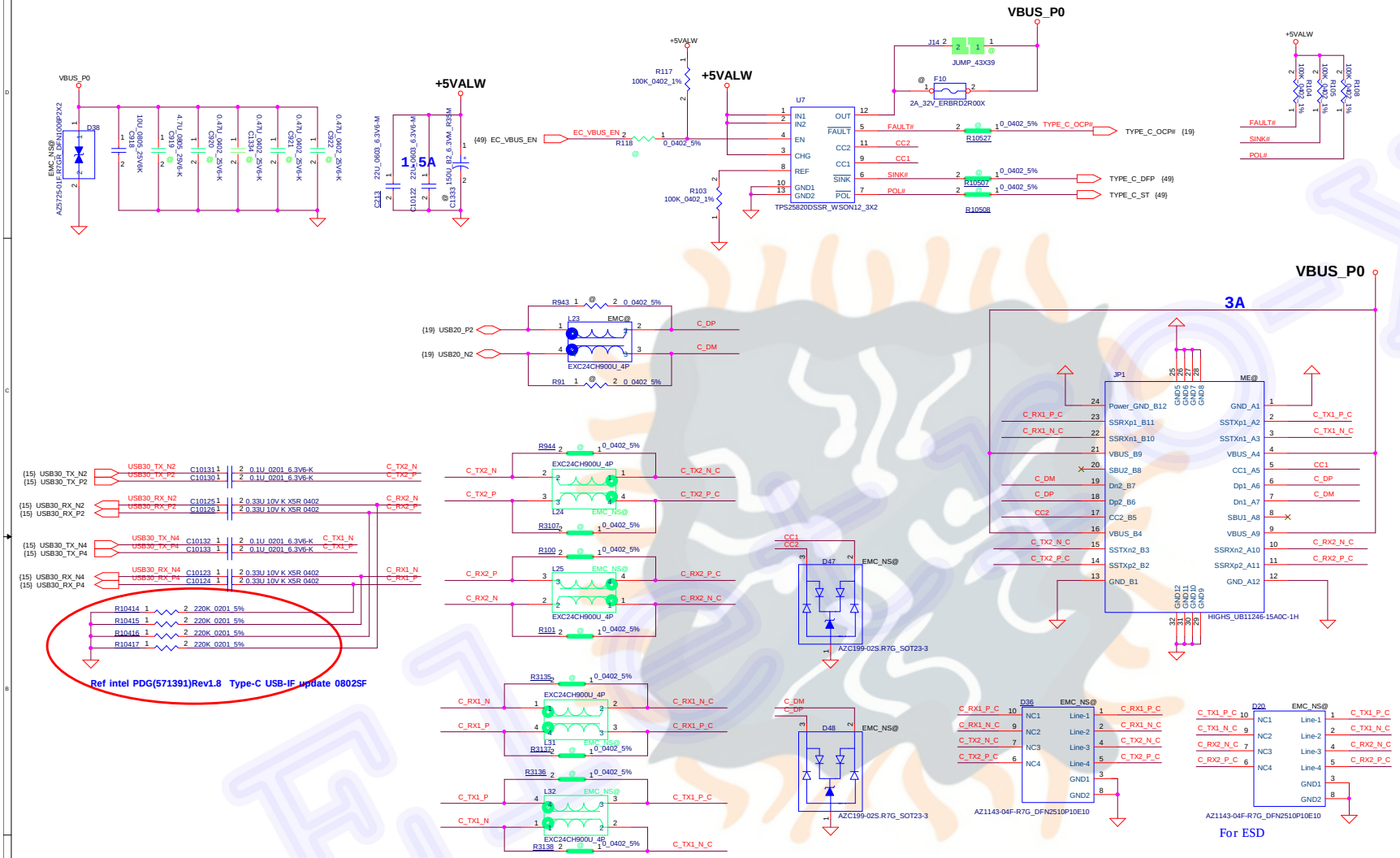
Title: **HDD/ODD CONN**

Size: Custom | Document Number: **FG541/FG741** | Rev: 0.1

Date: Thursday, January 03, 2019 | Sheet 47 of 69

Eletro-X



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

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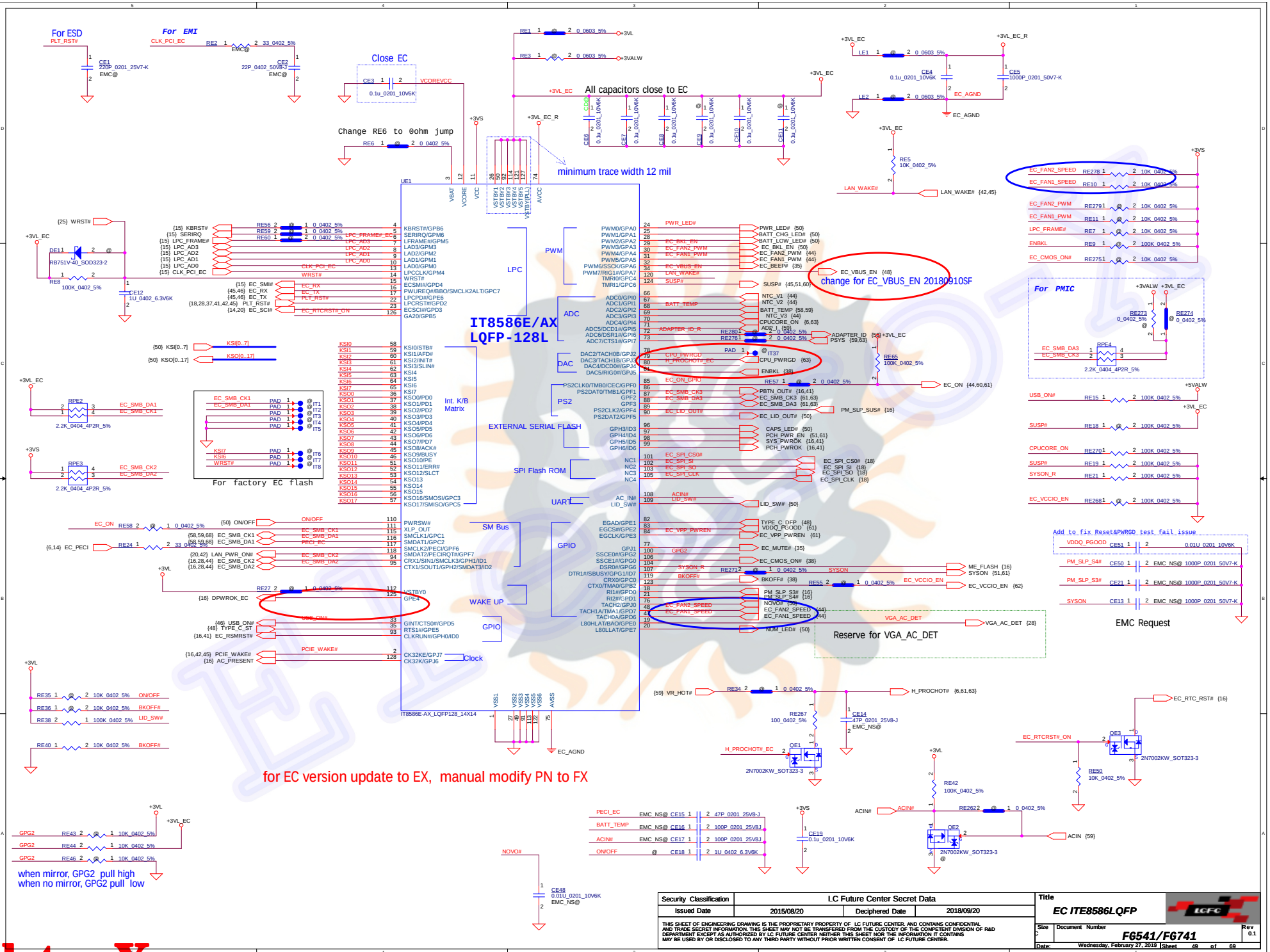
Title: 3D Camera

Size: C | Document Number: FG541/FG741 | Rev: 0.1

Date: Friday, March 01, 2019 | Sheet 48 of 69

Eletro-X


IT8586E/AX
LQFP-128L
UE1
For ESD
For EMI
Close EC
Change RE6 to 0ohm jump
All capacitors close to EC
minimum trace width 12 mil
change for EC_VBUS_EN 20180910SF
For PMIC
For factory EC flash
Reserve for VGA_AC_DET
EMC Request
Add to fix Reset&PWRGD test fail issue
for EC version update to EX, manual modify PN to FX
when mirror, GPG2 pull high
when mirror, GPG2 pull low
LPC
PWM
ADC
DAC
PS2
EXTERNAL SERIAL FLASH
SPI Flash ROM
UART
GPIO
SM Bus
WAKE UP
Clock
Int. K/B Matrix
IT8586E-AX_LQFP128_14X14
Security Classification
LC Future Center Secret Data
Issued Date
2015/08/20
Deciphered Date
2018/09/20
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Title
EC ITE8586LQFP
Size
C
Document Number
FG541/FG741
Rev
0.1
Date:
Wednesday, February 27, 2019
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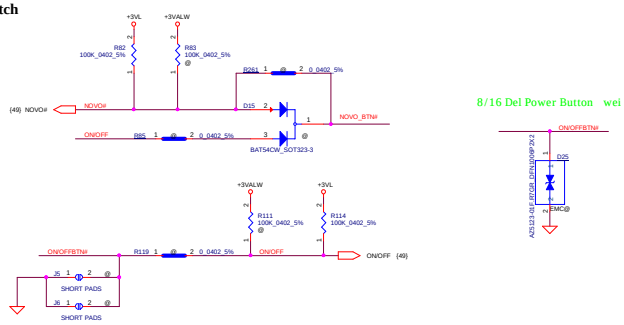
of
69

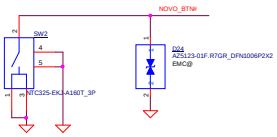
Eletro-X

ON/OFF switch



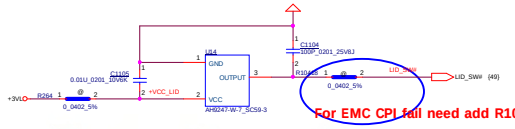
8/16 Del Power Button wei

Novo button



8/31 Update the P/N SN100008W00 wei

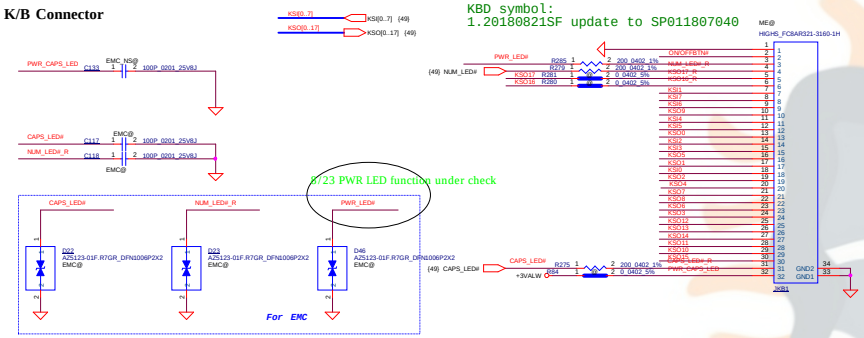
LID switch



For EMC CPI fail need add R10418---1204SF

K/B Connector

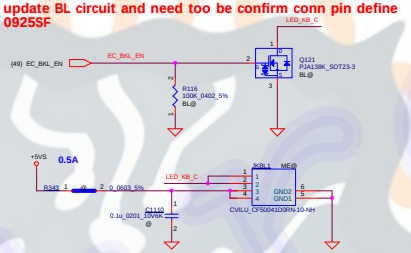
KBD symbol:
1.20180821SF update to SP011807040



8/23 PWR LED function under check

KB Backlight Connector

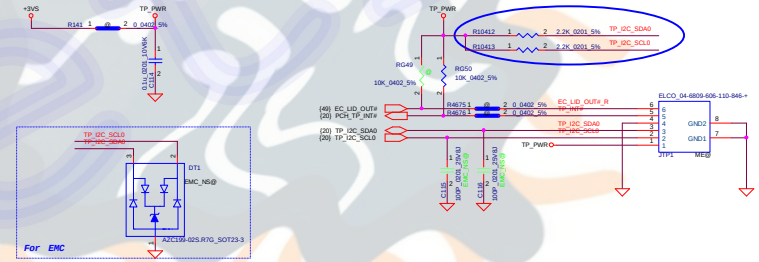
update BL circuit and need too be confirm conn pin define
0925SF

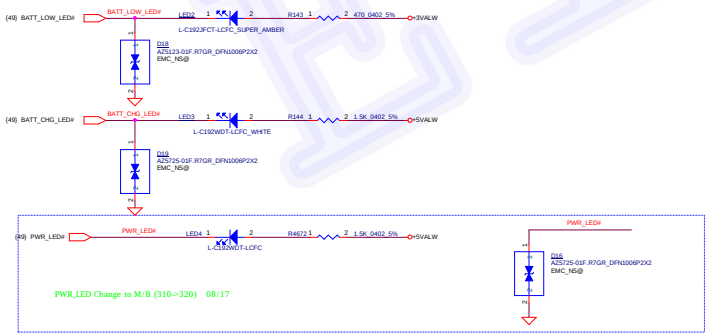


Finger Print Connector

follow OD V1.5 delete finger print function
0927SF

TP/B Connector





PWR_LED Change to M/B (310->320) 08/17

Security Classification	LC Future Center Secret Data		Title	KBD/PWR/IO/LED/TP Conn
Issued Date	2015/08/20	Deciphered Date 2018/09/20		

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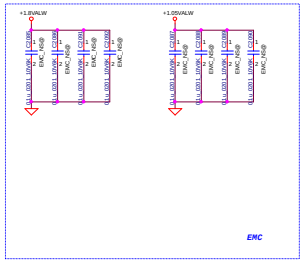
Eletro-X

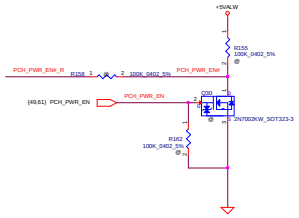
delete Load Switch 5VS and 3VS 20181101SF

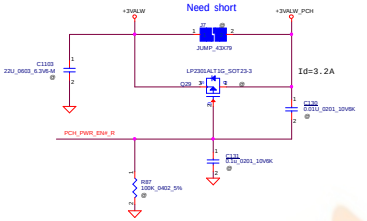
Load Switch
+5VALW To +5VS
+3VALW To +3VS

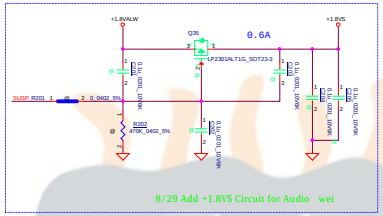
+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms

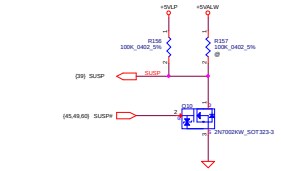
VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm



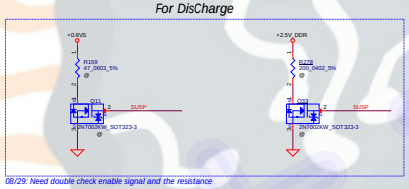






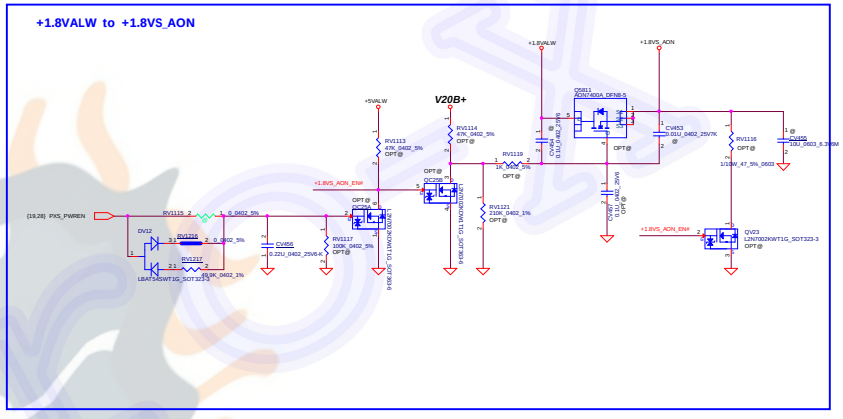


For DisCharge



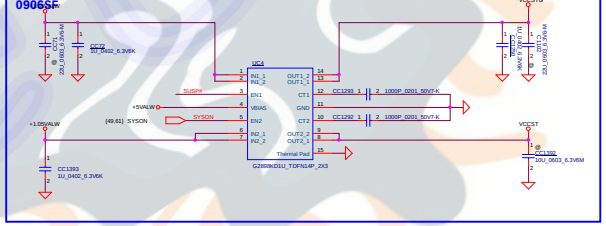
08/29: Need double check enable signal and the resistance

+1.8VALW to +1.8VS_AON

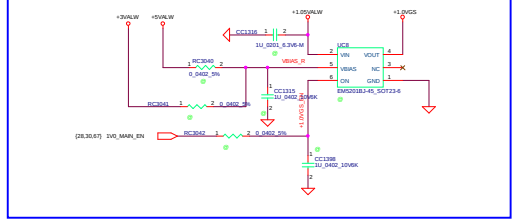


delete reserved for VCCSTG & VCCST 0928SF

VCCSTG & VCCST change to Dual Switch 0906SF



+1.0VALW TO +1.0VGS



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2018/09/20

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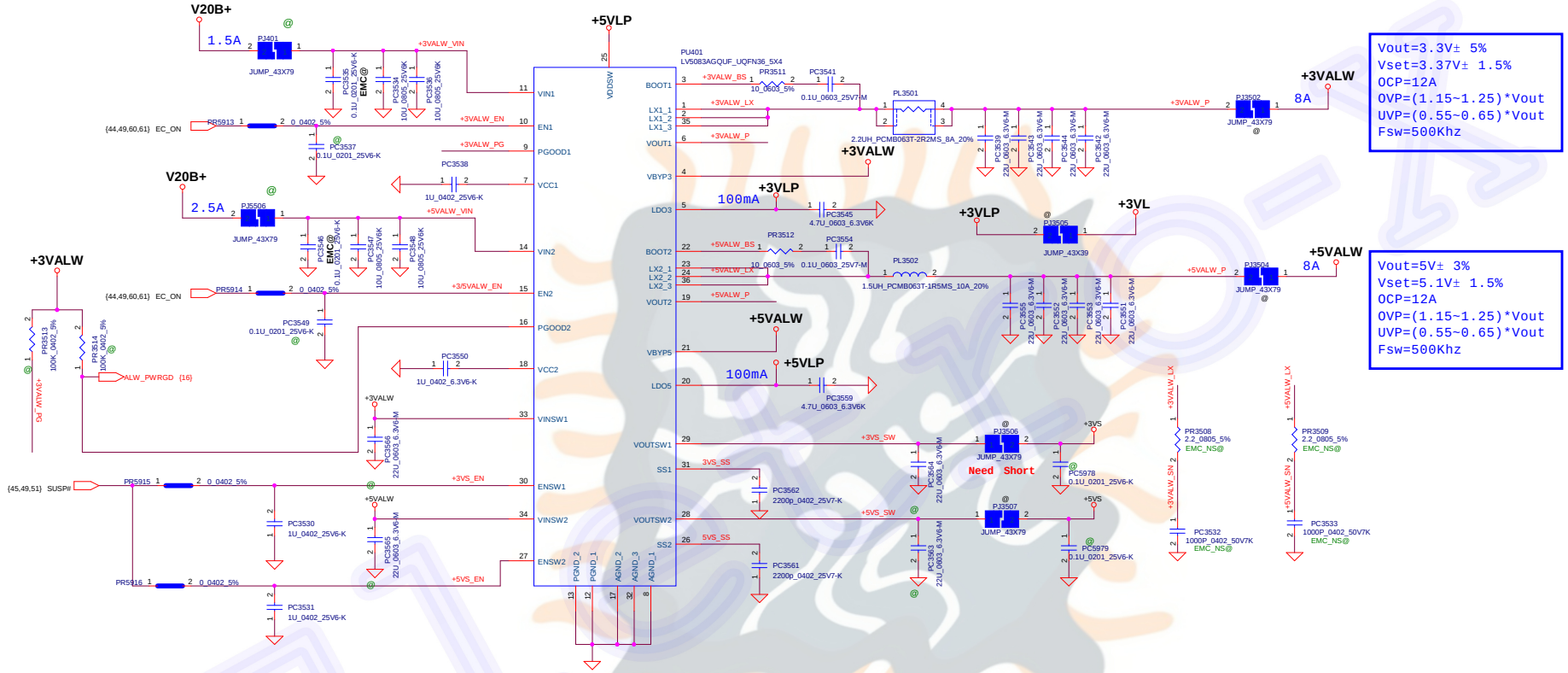
Title: DC V TO VS INTERFACE

Size: Custom | Document Number: F6541/F6741 | Rev: 0.1

Date: Wednesday, February 27, 2019 | Sheet 31 of 69

Eletro-X



Vout=3.3V± 5%
Vset=3.37V± 1.5%
OCP=12A
OVP=(1.15~1.25)*Vout
UVP=(0.55~0.65)*Vout
Fsw=500Khz

Vout=5V± 3%
Vset=5.1V± 1.5%
OCP=12A
OVP=(1.15~1.25)*Vout
UVP=(0.55~0.65)*Vout
Fsw=500Khz

VOUT=3.07V
TDC=6A
OCP=10A
Fsw=600Khz

VOUT=5.01V
TDC=8A
OCP=12A
Fsw=600Khz

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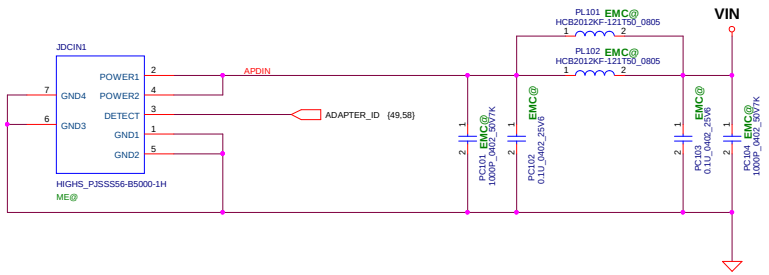
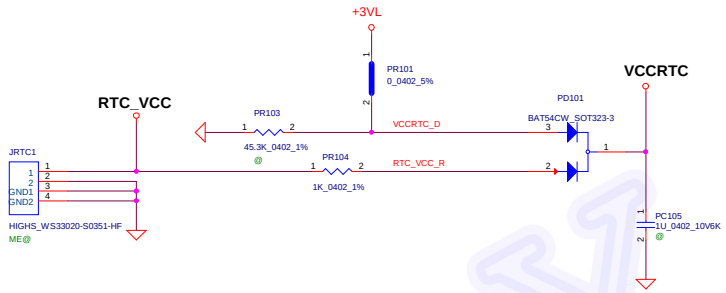
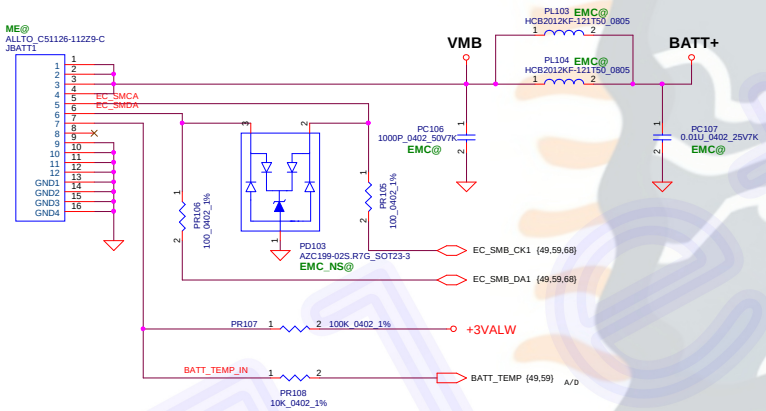
Eletro-X



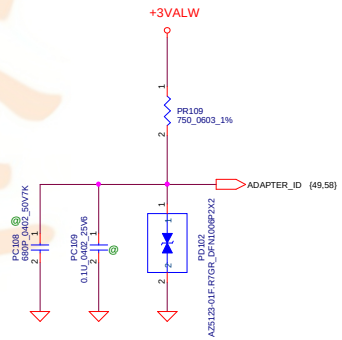
DC IN:1.DC IN connect apply for PN HIGHS_PJSSS56-B5000-1H_5P-T ,need replace connector rate current 7A



RTC:1. 0ohm delete
2.the max VCCRTC < 3.2V specification
3.RTC cable 35mm



battery IN:
1.20180821SF update to SP011808066
2.battery connector 12pin per pin 4.5A



ADP_ID:1. cost down solution
2.EC initial ID function

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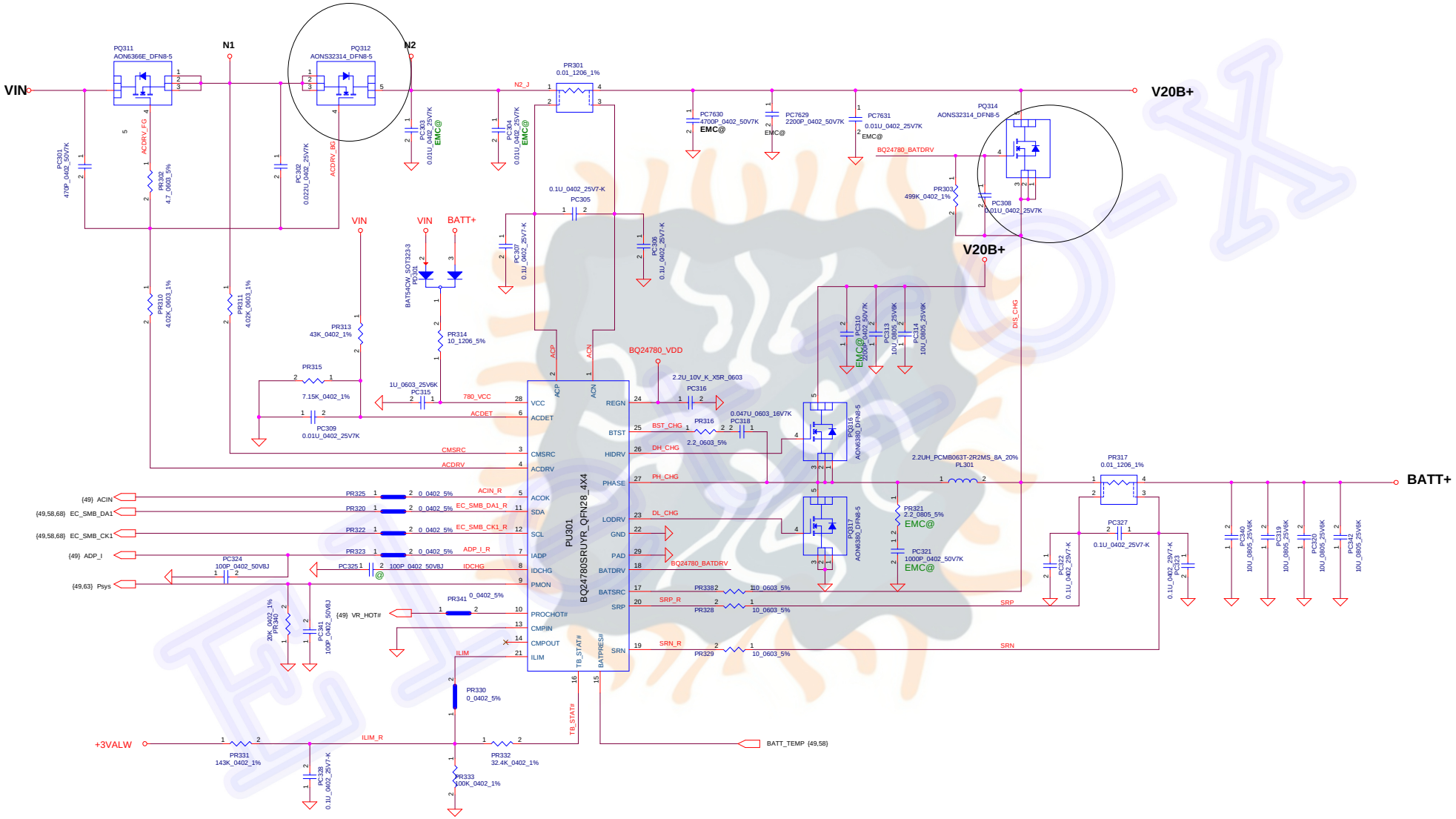

charge current:1C 5A
charge voltage:12.6V
charge frequency:800K
ILIM pin:charge7A, turbo-discharge-10A

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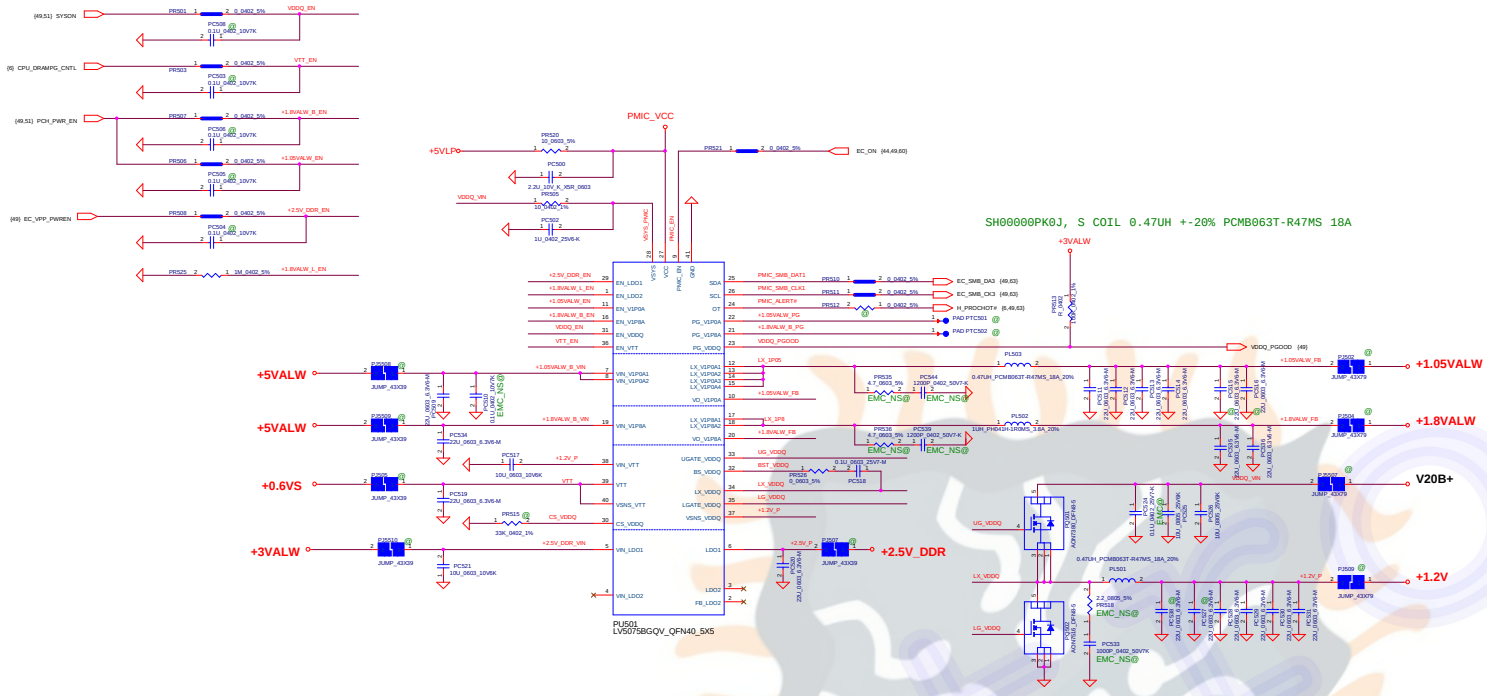

1.2V: setting 1.21V
TDC:8A
OCP:125mV/25A
OVP:120%
frequency:1Mhz
0.47UH_PCMC063T-R47MN_17.5A_20% DCR no limit
1.05V: setting 1.05V
TDC:6A
OCP:10A
OVP:120%
frequency:1Mhz
1.8V: setting 1.81V
TDC:3A
OCP:6A
OVP:120%
frequency:1Mhz

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Title: Cover Page

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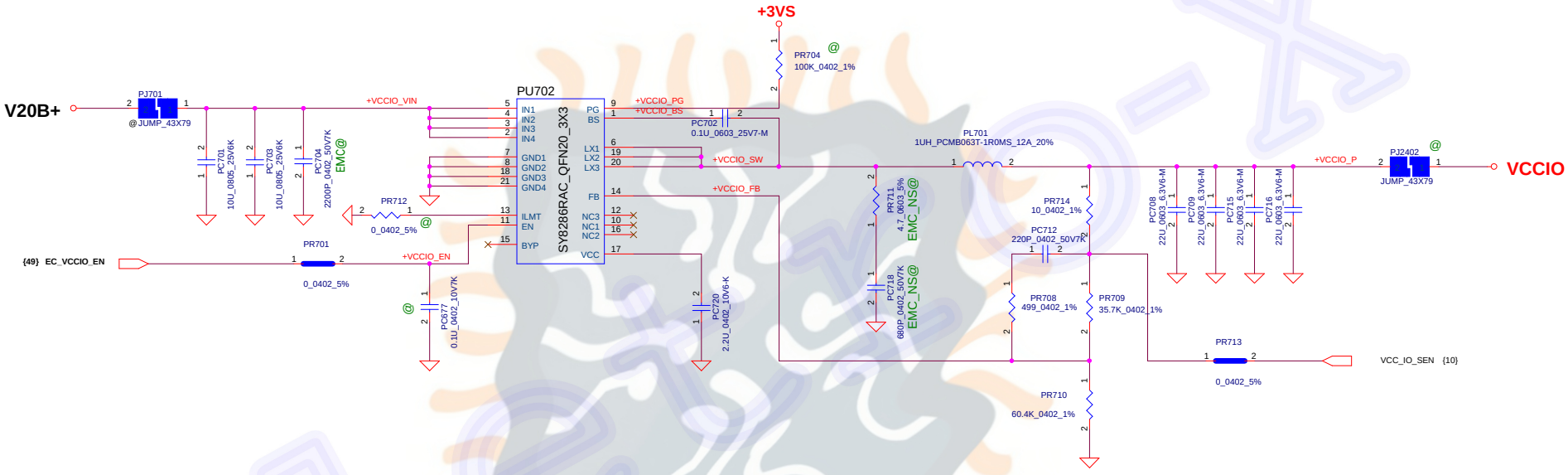

VCCIO:FB=0.6V/0.954V
TDC=6A
OCP:10A
OVP:120%
frequency:500Khz
remove sense pull high in power side

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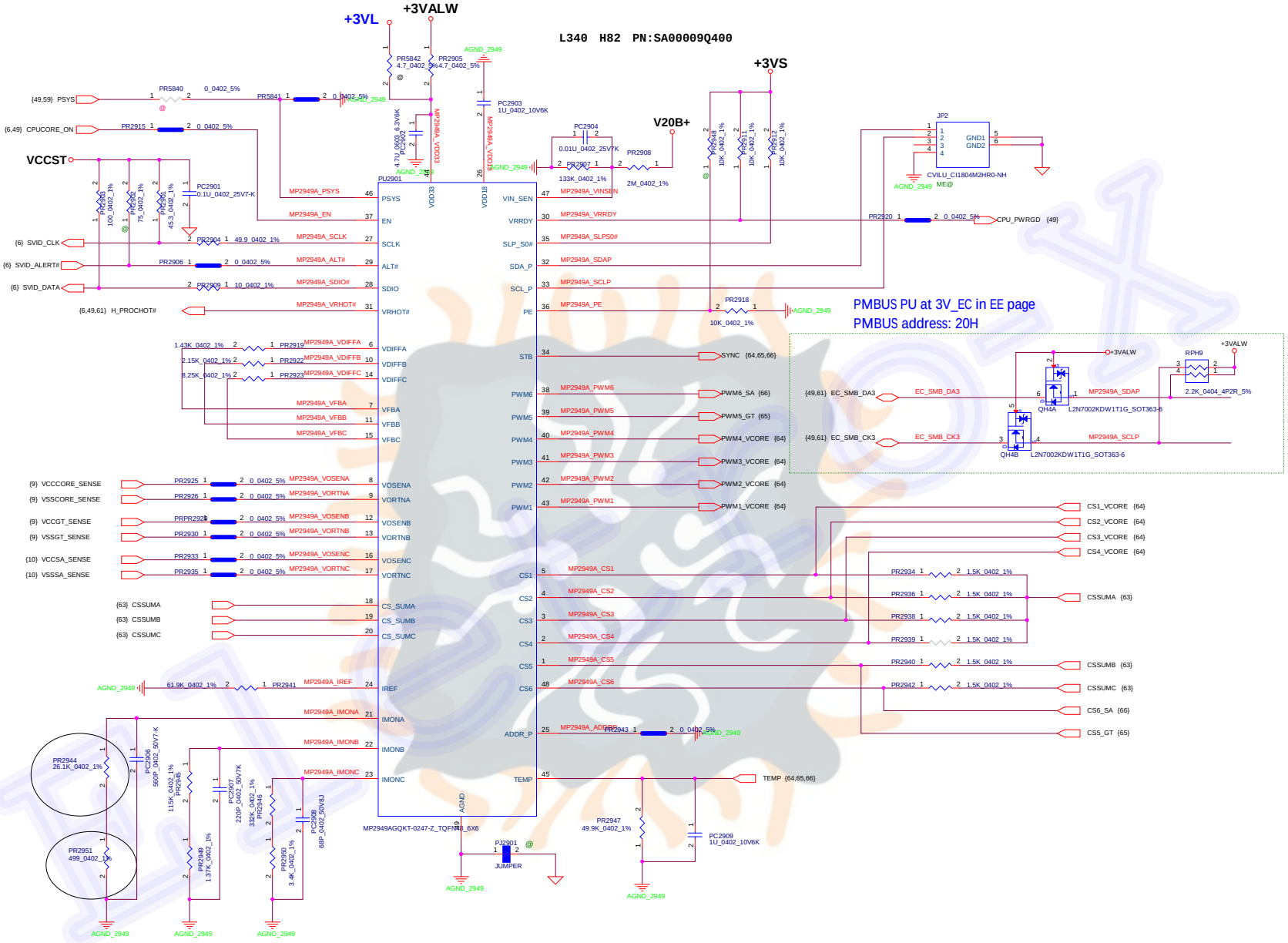

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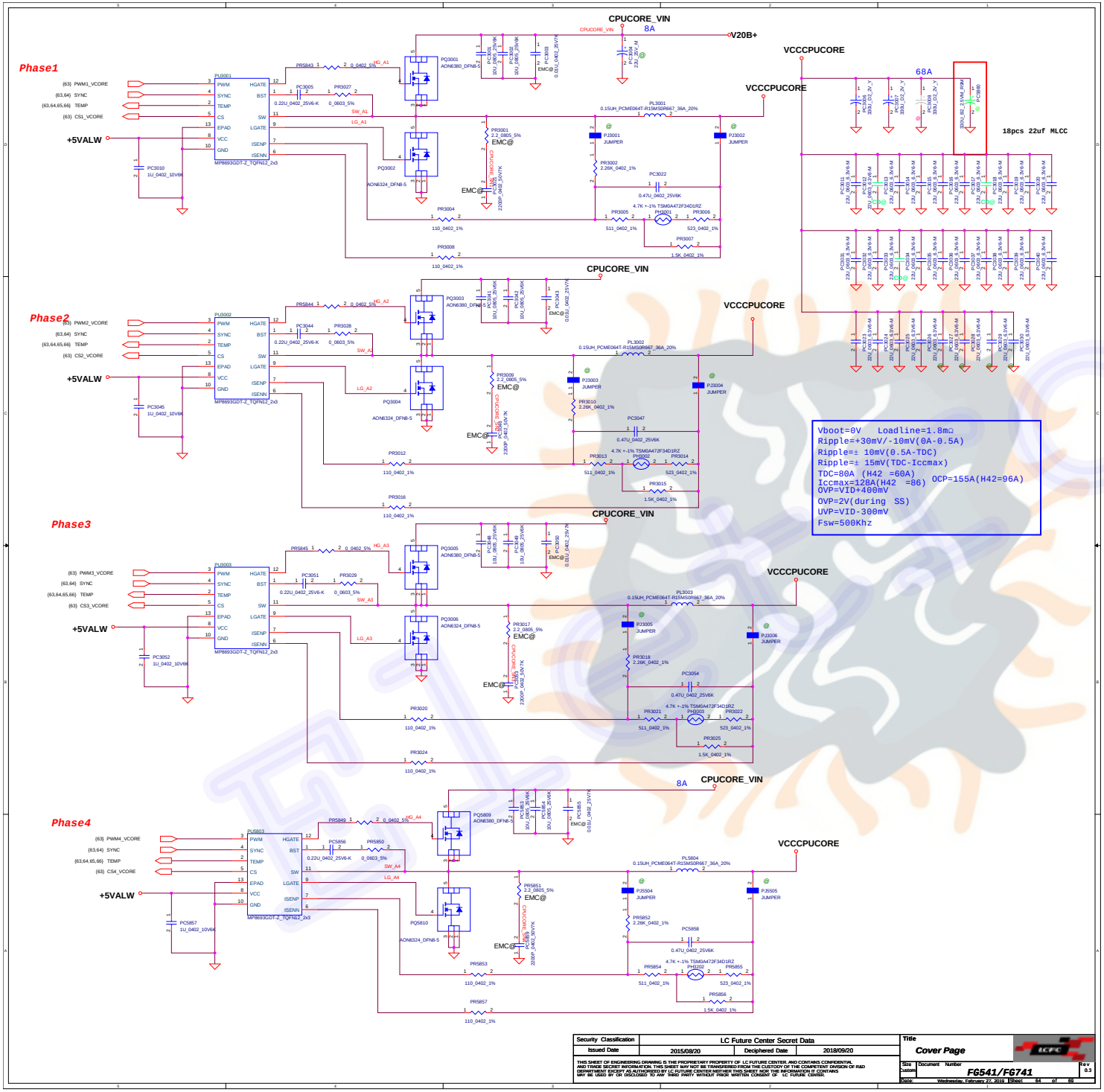

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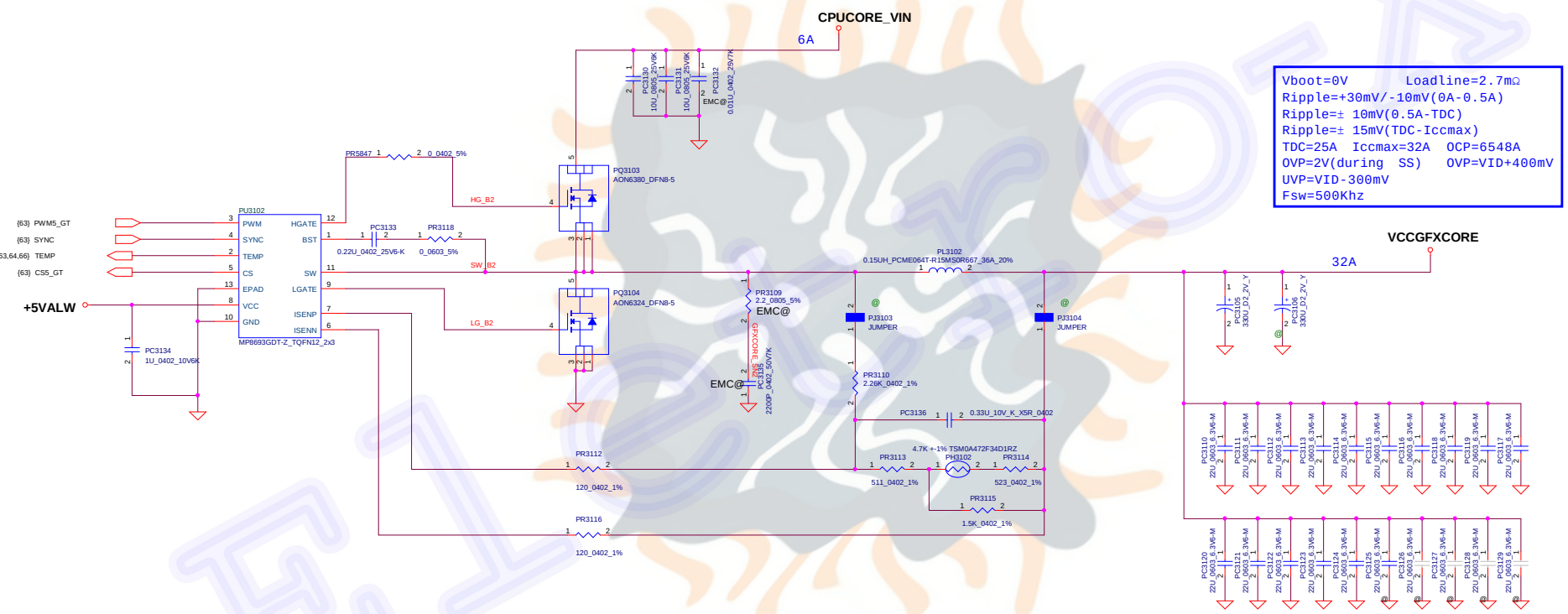

Vboot=0V Loadline=2.7mΩ
Ripple=+30mV/-10mV(0A-0.5A)
Ripple=± 10mV(0.5A-TDC)
Ripple=± 15mV(TDC-Iccmax)
TDC=25A Iccmax=32A OCP=6548A
OVP=2V(during SS) OVP=VID+400mV
UVP=VID-300mV
Fsw=500Khz

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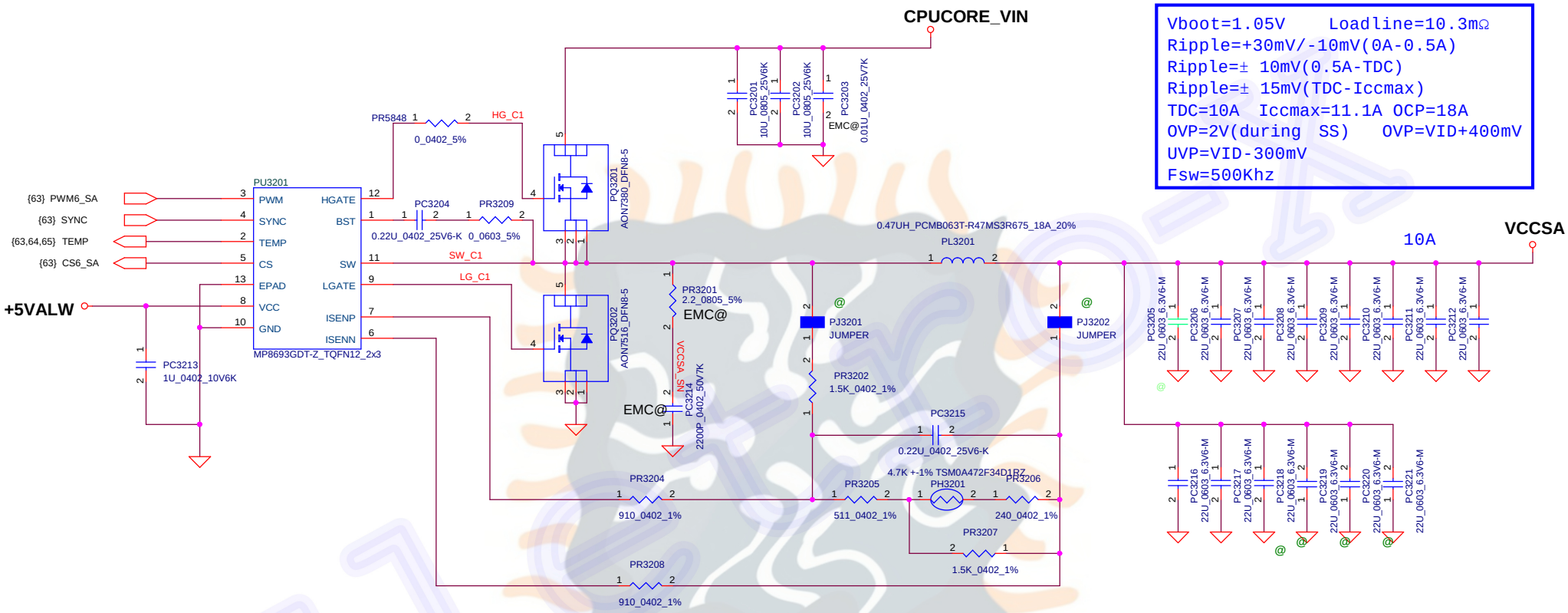

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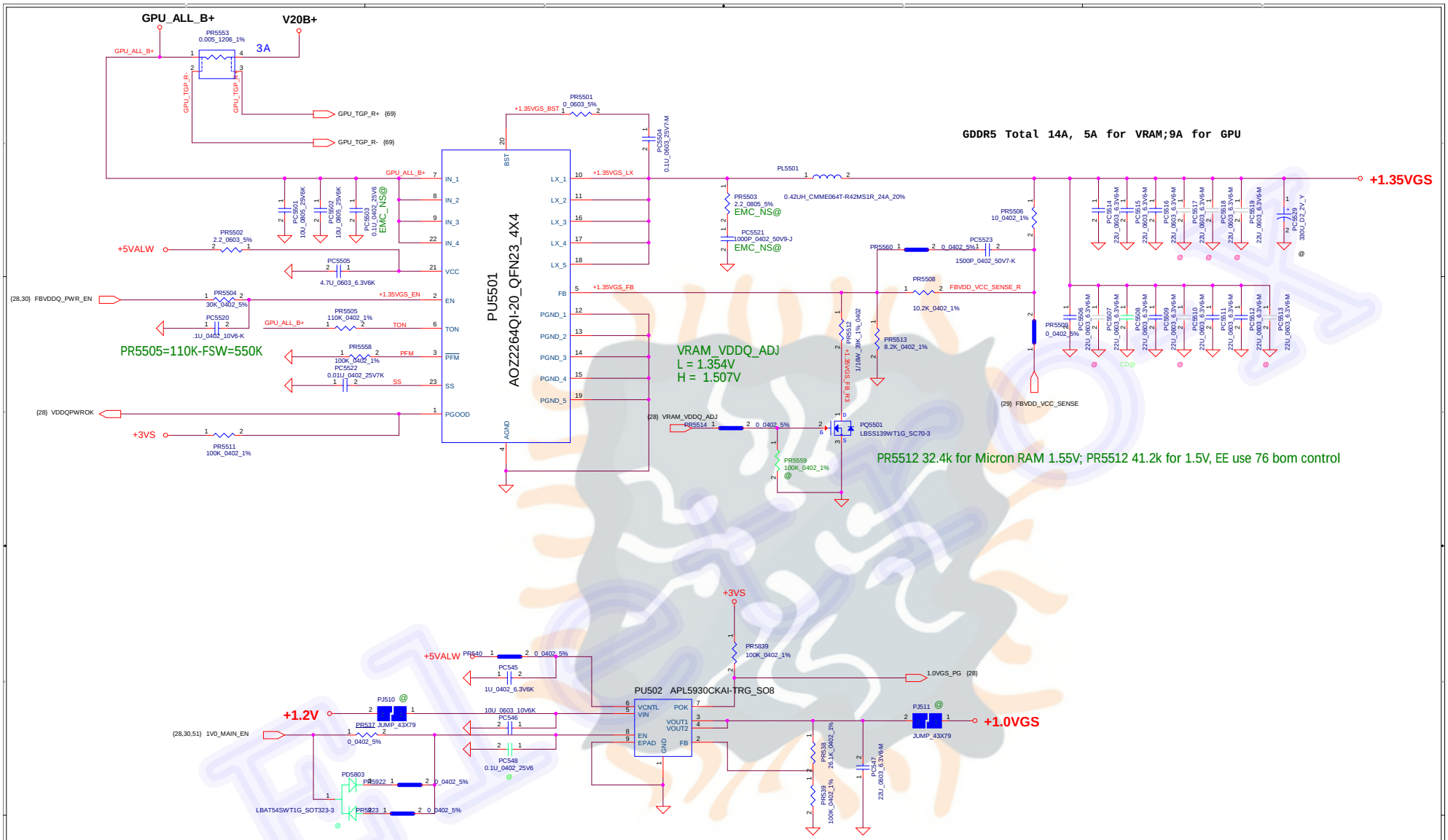

1.35VGS
FB:0.6V/1.35V
TDC=11A
ICCMAX=20A
OCP=25A
FSW=550K

LDO-1.0VGS
TDC:1A
iccmax:1.1A
FB:0.8V/1.0V

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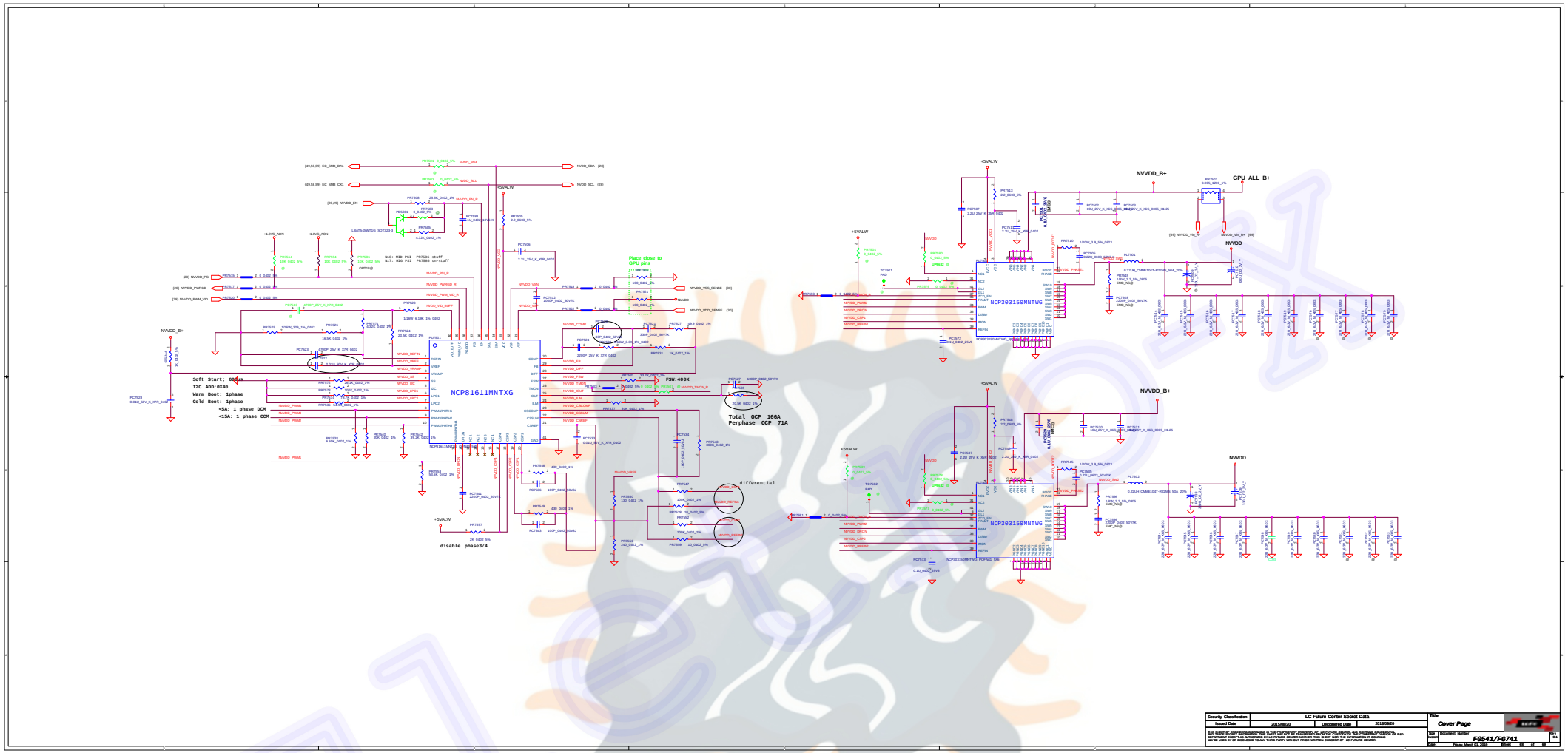
NCP81611MNTXG
NCP303150MNTWG
NCP303150MNTWG
Soft Start; 60us
I2C ADD:0X40
Warn Boot: 1phase
Cold Boot: 1phase
<5A: 1 phase DCM
<15A: 1 phase CCM
disable phase3/4
Place close to GPU pins
FSW:400K
Total OCP 166A
Perphase OCP 71A
differential
NVVDD_B+
GPU_ALL_B+
NVVDD
+5VALW
Security Classification
LC Future Center Secret Data
Issued Date
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Deciphered Date
2015/09/20
Title
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Size
Document Number
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0.1
Date: Friday, March 06, 2015
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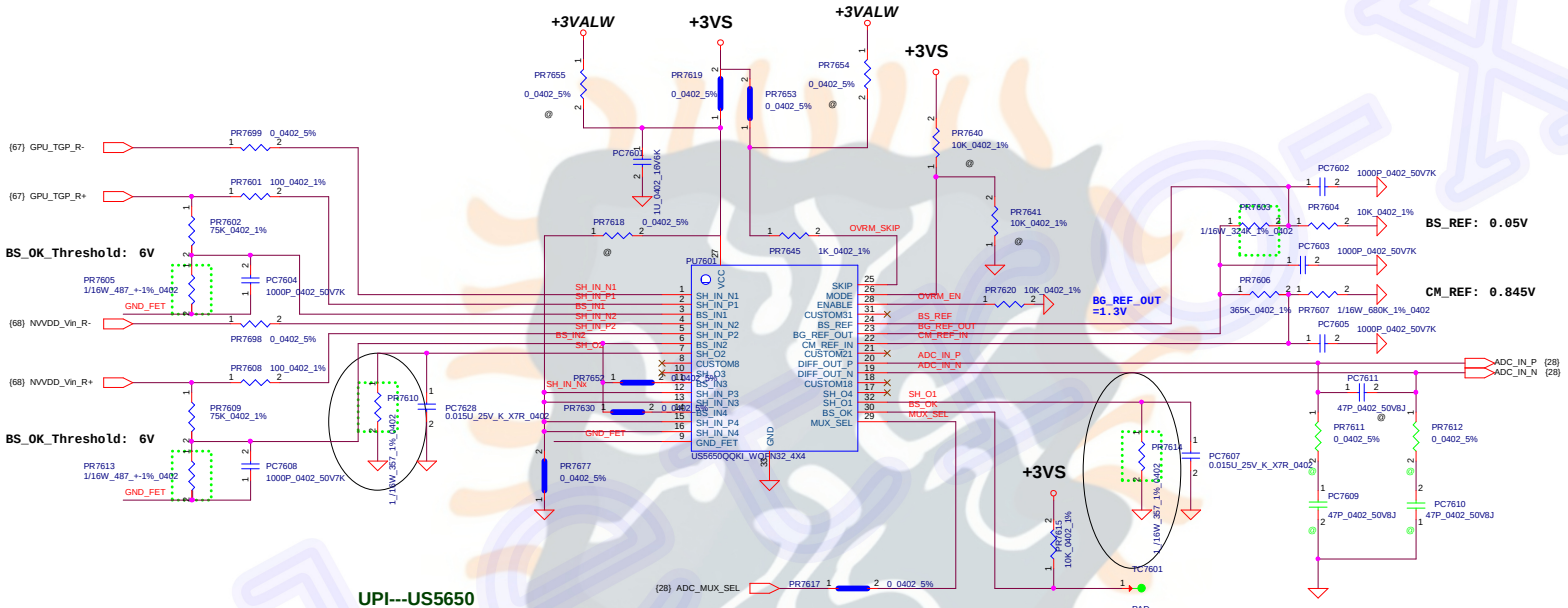

UPI---US5650
PR7605=487
PR7613=487
PR7610=357ohm for Lower 70W 215 for 75W to 90W 165 for 100W to 110W
PR7614=357ohm for Lower 70W 215 for 75W to 90W 165 for 100W to 110W
PR7603=324K
PR7602=75K
PR7609=75K
PC7604=1nF
PC7608=1nF

ON---NCP45491
PR7605=649
PR7613=649
PR7610=475ohm for lower 70W 287 for 75W to 90W 221 for 100W to 110W
PR7614=475ohm for lower 70W 287 for 75W to 90W 221 for 100W to 110W
PR7603=243K
PR7602=75K
PR7609=75K
PC7604=1nF
PC7608=1nF

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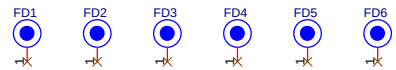
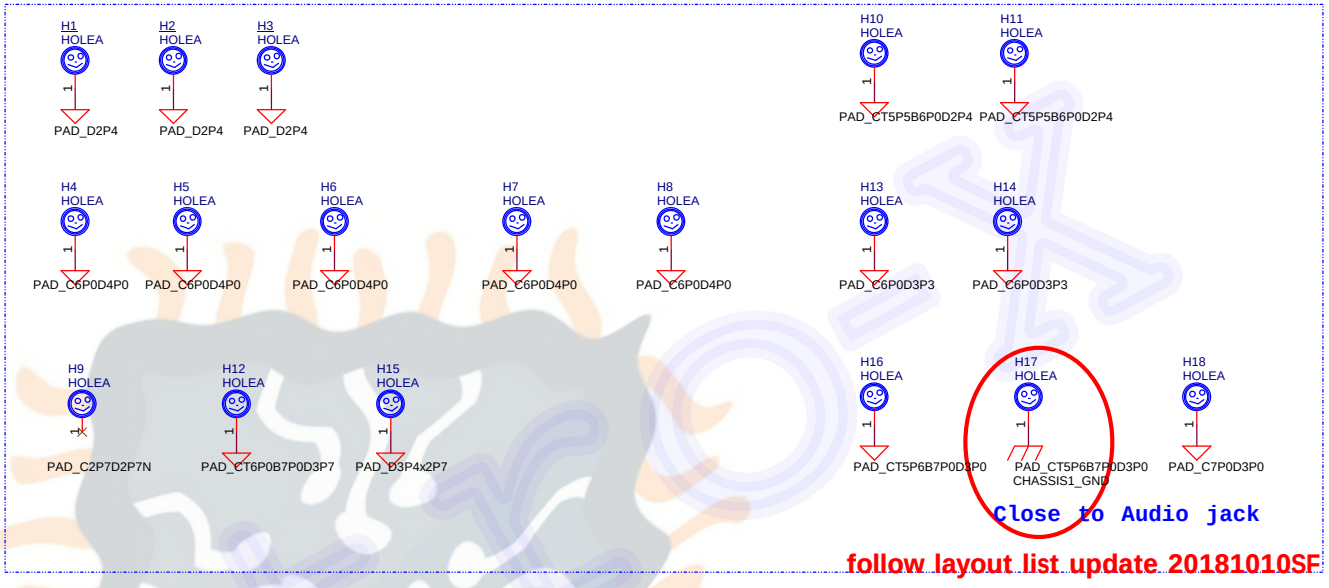
Eletro-X

GPU Thermal Holex2 Close to RJ45 DC-IN x2

CPU Thermal Holex3 WLAN Standoff

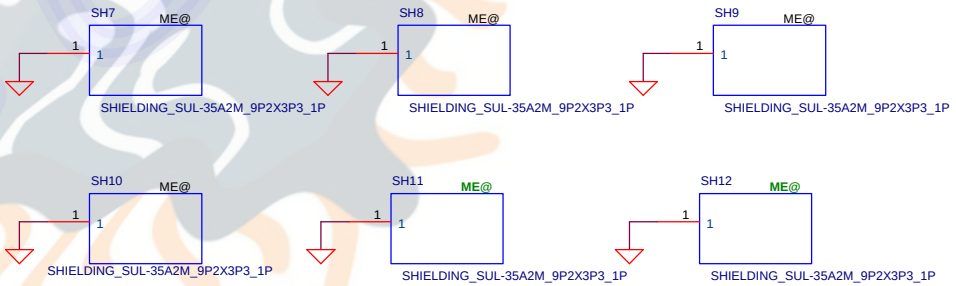
PCB Fedical Mark PAD





Close to Audio jack

follow layout list update 20181010SF



USB3.0 Shielding

DDR4 Shielding

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Title: Hole

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Eletro-X

N17P-G1 GPIO

GPIO	I/O	ACTIVE	Function Description	I/O Termination
GPIO0	OUT	-	PWM Output to control NVVDD	
GPIO1	OUT	-	FB Enable for GC6 2.1	
GPIO2	IN	-	GPU wake signal for GC6 2.1	
GPIO3	OUT	-	PWM Output to control the SRAM power supply	
GPIO4	OUT	-	GPU power sequencing for GC6 2.1 --- 1V8_MAIN_EN	
GPIO5	IN	N/A	Active low Frame Lock	
GPIO6	OUT	-	Phase Shedding, NVVDD_PSI	
GPIO7	OUT	N/A	Panel Backlight enable	
GPIO8	OUT	-	Memory voltage Control	
GPIO9	I/O	-	Active Low Thermal Alert	
GPIO10	OUT	-	Memory VREF Control (100K pull Down)	
GPIO11	OUT	-	Panel Power enable	
GPIO12	IN	-	AC power detect or power supply overdraw input	(10K pull High)
GPIO13	OUT	N/A	LCD Panel Backlight Enable	
GPIO14	IN	N/A	Hot Plug Detect for IFPA	
GPIO15	IN	N/A	Hot Plug Detect for IFPB	
GPIO16	OUT	-	System side PCIe reset monitor	
GPIO17	IN	N/A	Hot Plug Detect for IFPD	
GPIO18	IN	N/A	Hot Plug Detect for IFPE	
GPIO19	OUT	N/A	3D Vision L/R Signal	
GPIO20		N/A	GC5_MODE	
GPIO21	I/O	N/A	UNUSED	
GPIO22	I/O	N/A	UNUSED	
GPIO23	OUT	-	GPU PCIe self-reset control	
GPIO24	IN	N/A	Hot Plug Detect for IFPF	
GPIO25		N/A	UNUSED	
GPIO26		N/A	UNUSED	
GPIO27	IN	N/A	Hot Plug Detect for IFPC	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111

H=High: Tied to 1.8V
M=Middle: Tied to 0.9V
L=Low: Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
L	L	L	1111 DEFAULT
L	L	H	1110
L	H	L	1101
L	H	H	1100
H	L	L	1011
H	L	H	1010
H	H	L	1001
H	H	H	1000
L	L	M	0111
L	M	L	0110
L	M	H	0101
L	H	M	0100
H	L	M	0011
H	M	L	0010
H	M	H	0001
H	H	M	0000

1:ENABLE 0:DISABLE

SOR0/1/2/3 ENABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

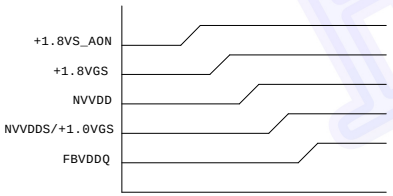
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

N17P-G1 Power Sequence

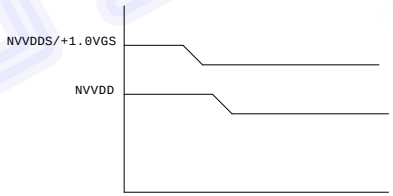


1. All power rail ramp up time should be larger than 40us and is recommended to be less than 2ms.

2. T (from 1V8_MAIN_EN to PEX_DVDD/NVVDD_Pgood) must NOT exceed 4ms.

3. All 3.3V devices that connect to the GPU must be powered after 1V8_AON; GPU can NOT have any 3.3V leakage path before 1V8_AON present.

4. The previous power rail must ramp up to 90% before the next power rail can start ramping up.



1. NVVDDS/PEX_DVDD must ramp down before NVVDD, all other power rails can ramp down together with NVVDD.

2. All 3.3V devices that connect to the GPU must be ramp down before 1V8_AON; GPU can NOT have any 3.3V leakage path after 1V8_AON and 1.8V_MAIN power down.

3. The previous power rail must ramp down to 10% before the next power rail can start ramping down.

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Title: VGA Notes List

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